TC518128AP/ASP/AF/AFW-80,-10,-12
TC518128APL/ASPL/AFL/AFWL/AFTL/ATRL-80,-10,-12

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518128A Family is a 1M bit high speed CMOS Pseudo Static RAM organized as 131,072 words by 8 bits. The TC518128A Family utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. The feature includes single power supply of 5V±10%. The $\overline{RFSH}$ input allows two types of refresh operation - auto refresh and self refresh. The TC518128A Family also features static RAM like write function that the input data is written into the memory cell at the rising edge of R/W, thus being easy to interface with microprocessor.

The TC518128A Family is a pin - compatible with 1M bit CMOS Static RAM - JEDEC standard and is moulded in a 32 pin standard 0.6 inch and 0.3 inch width plastic DIP and small - out line plastic flat package and a 32 pin plastic thin small - out - line package (forward, reverse type).

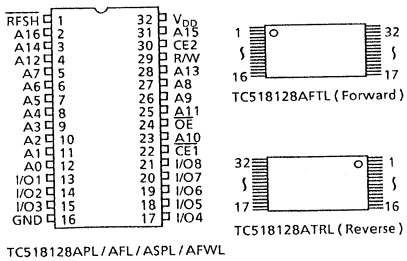
FEATURES

- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation
- Single Power Supply : 5V±10%
- Auto refresh is capable by internal counter.
- Self refresh is capable by internal timer.

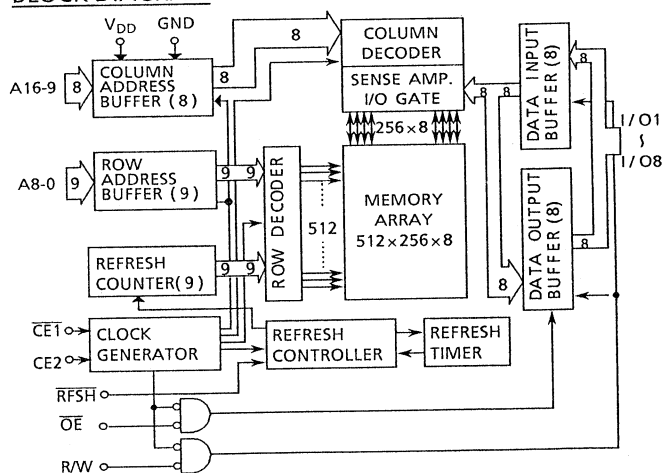
	TC518128A Family		
	- 80	- 10	- 12
t_{CEA} CE Access Time	80ns	100ns	120ns
t_{OEA} OE Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA / 200μA (L version)		

- All inputs and outputs : TTL compatible
- 512 refresh cycle / 8ms
- Auto refresh power down function
- Pin Compatible : 1M SRAM (JEDEC)
- Logic Compatible : SRAM R/W Pin
- Logic Compatible : SRAM R/W Pin
- Package: TC518128AP / APL : DIP32-P-600
  TC518128AF / AFL : SOP32-P-450
  TC518128ASP / ASPL : DIP32-P-300B
  TC518128AFW/AFWL : SOP32-P-525
  TC518128AFTL : TSOP32-P-0820
  TC518128ATRL : TSOP32-P-0820A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0~A16	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1~I/O8	Data Inputs / Outputs
V_{DD}	Power
GND	Ground

(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	$\overline{RFSH}$	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

FUNCTION LOGIC

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
L	H	L	H	*	V*	OUT	Read
L	H	*	L	*	V*	IN	Write
L	H	H	H	*	V*	HZ	CE only Refresh
H	*	*	*	L	*	HZ	Auto/Self Refresh
*	L	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by
*	L	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE1}$ falling edge (CE2 = H) or CE2 rising edge ($\overline{CE1}$ = L), all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	− 1.0~7.0	V	1
V_{OUT}	Output Voltage	− 1.0~7.0	V	
V_{DD}	Power Supply Voltage	− 1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	− 55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	− 1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE1}$, CE2, Address cycling: t_{RC} = t_{RC} min.	80ns version	–	50	70	mA	3, 4
		100ns version	–	40	60		
		120ns version	–	35	50		
I_{DDS1}	Standby Current $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} $\overline{RFSH}$ = V_{IH}	Normal version	–	–	2	mA	
		L version	–	–	1		
I_{DDS2}	Standby Current $\overline{CE1}$ = V_{DD} – 0.2V or CE2 = 0.2V, $\overline{RFSH}$ = V_{DD} – 0.2V	Normal version	–	–	1	mA	
		L version	–	100	200	μA	
I_{DDF1}	Self Refresh Current (Average Current) $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, $\overline{RFSH}$ = V_{IL}	Normal version	–	–	2	mA	
		L version	–	–	1		
I_{DDF2}	Self Refresh Current (Average Current) $\overline{CE1}$ = V_{DD} – 0.2V or CE2 = 0.2V, $\overline{RFSH}$ = 0.2V	Normal version	–	–	1	mA	
		L version	–	100	200	μA	
I_{DDF3}	Auto Refresh Current (Average Current) ($\overline{RFSH}$ cycling : tFC = tFC min)		–	–	2	mA	
I_{DDF4}	CE only Refresh Current (Average Current) ($\overline{CE1}$, CE2, Address cycling : tRC = tRC min)	80ns version	–	50	70	mA	3
		100ns version	–	40	60		
		120ns version	–	35	50		
$I_{I(L)}$	Input Leakage Current 0V ≦ V_{IN} ≦ V_{DD}, All other Inputs not under test = 0V		– 10	–	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≦ V_{OUT} ≦ V_{DD}		– 10	–	10	μA	
V_{OH}	Output High Level I_{OH} = – 5mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA		–	–	0.4	V	

Note) In I_{DDS1} and I_{DDF1} with $\overline{CE1}$ = V_{IH} (CE2 = V_{IL}), these specification limits are guaranteed under the condition of CE2 = V_{IH} or CE2 = V_{IL} ($\overline{CE1}$ = V_{IH} or $\overline{CE1}$ = V_{IL}). In I_{DDS2} and I_{DDF2} with $\overline{CE1}$ ≧ V_{DD} – 0.2V (CE2 ≦ 0.2V), theses specification are guaranteed under the condition of CE2 ≧ V_{DD} – 0.2V or CE2 ≦ 0.2V ($\overline{CE1}$ ≧ V_{DD} – 0.2V or $\overline{CE1}$ ≦ 0.2V).

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25 °C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE1}$, CE2, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	pF
C_{IO}	Input / Output Capacitance	–	7	pF

Note) This parameter periodically sampled is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

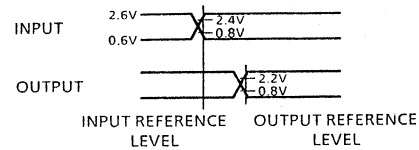
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	–	160	–	190	–	ns	
t_{RMW}	Read Modify Write Cycle Time	195	–	235	–	280	–	ns	
t_{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000	ns	13
t_P	CE Precharge Time	40	–	50	–	60	–	ns	
t_{CEA}	CE Access Time	–	80	–	100	–	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	–	50	ns	
t_{CLZ}	CE to Output in Low-Z	30	–	30	–	30	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	–	0	–	0	–	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{WP}	Write Pulse Width	60	–	70	–	85	–	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	–	35	–	45	–	ns	10
t_{DSC}	Data Set-Up Time from CE	30	–	35	–	45	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from CE	0	–	0	–	0	–	ns	10
t_{ASC}	Address Set-Up Time	0	–	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	20	–	25	–	30	–	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	–	15	–	15	–	ns	
t_{FC}	Auto Refresh Cycle Time	130	–	160	–	190	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	40	–	50	–	60	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
t_{FRS}	CE Delay Time form $\overline{RFSH}$ (Self Refresh)	160	–	190	–	225	–	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	–	8	–	8	–	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
t_{CES}	CE2 Low Set-Up Time	5	–	5	–	5	–	ns	14
t_{CEH}	CE2 Low Hold Time	5	–	5	–	5	–	ns	14

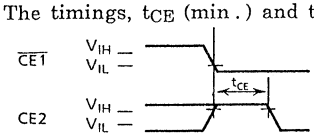
NOTES:

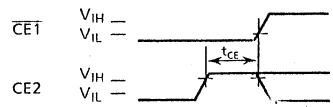
1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} and I_{DDF4} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE1}$ or low CE2 is required after power-up, before proper device operation is achieved.
6) AC measurements asuume t_T = 5ns.
7) Timing reference level

Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level:		V_{OH} = 2.2V
		V_{OL} = 0.8V

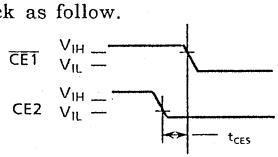


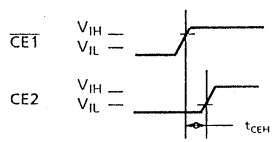
8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge and CE2 falling edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE1}$ and the rising edge of CE2. Therefore the all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}.
    Auto refresh : $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The timing parameter (t_{FRS}) must be kept for device proper operation in the following conditions.
    - after self refresh
    - in case of $\overline{RFSH}$ = "L" after power-up
13) The timings, t_{CE} (min.) and t_{CE} (max.), must be kept for device proper operation as follows.





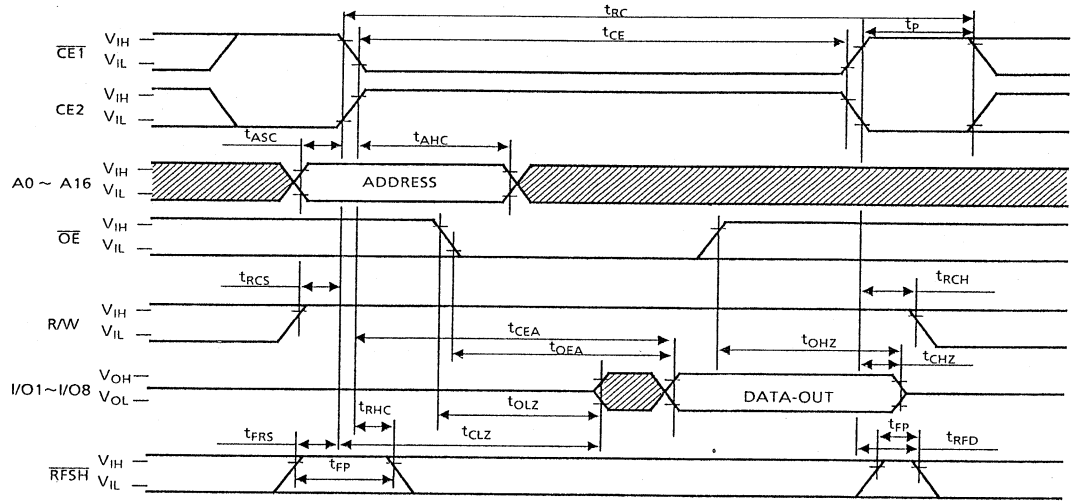
14) The timings, t_{CES} (min.) and t_{CEH} (min.), must be kept for useing $\overline{CE1}$ and CE2 at the same clock as follow.



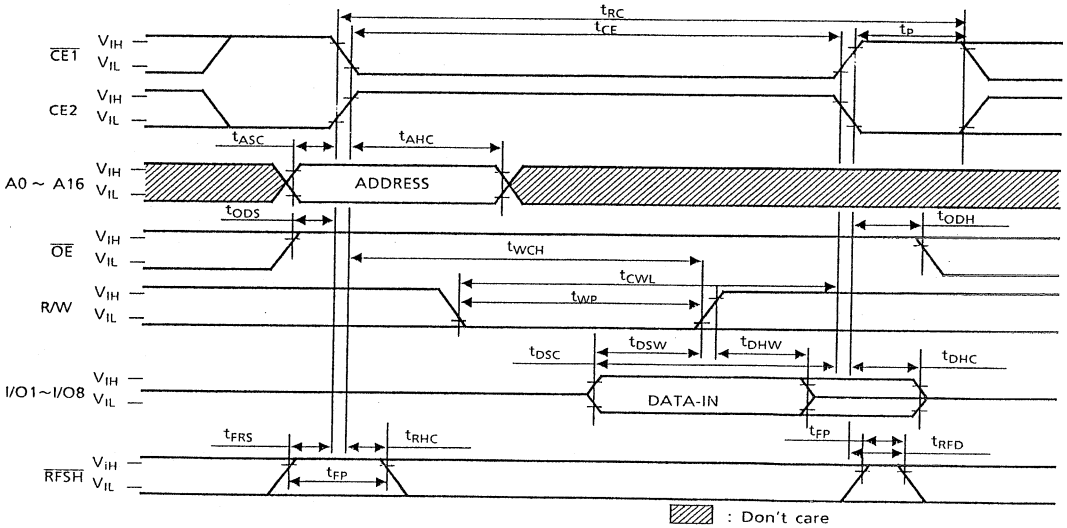


TIMING WAVEFORMS

READ CYCLE

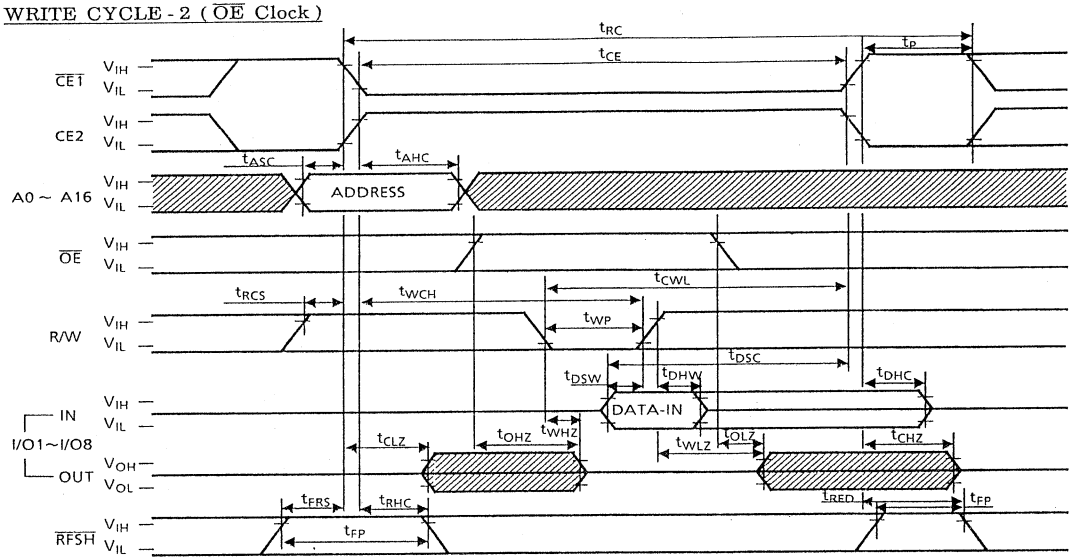


WRITE CYCLE-1 ($\overline{OE}$ Fix High)

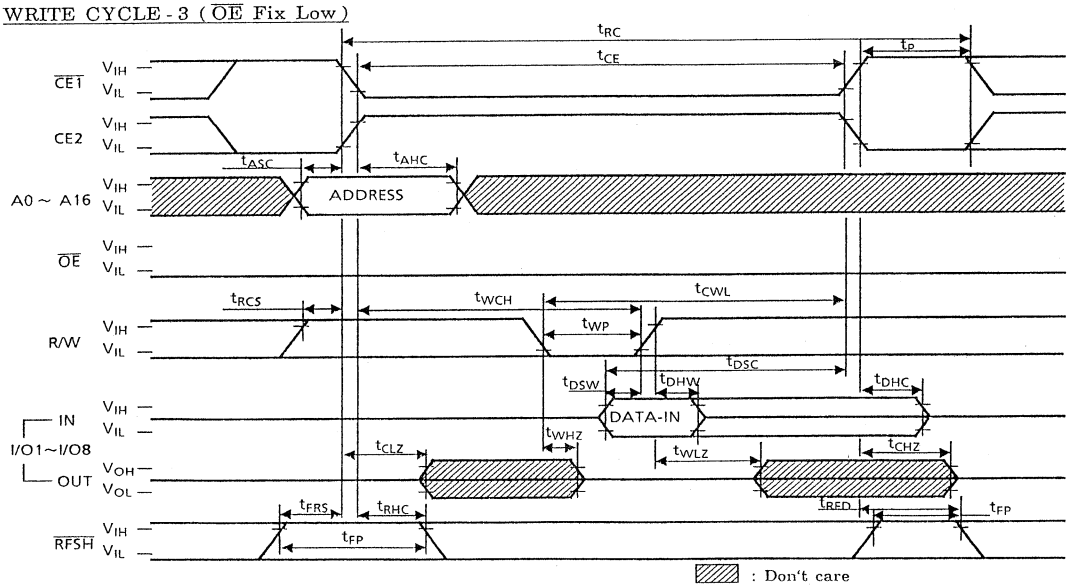


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

WRITE CYCLE - 2 ($\overline{OE}$ Clock)

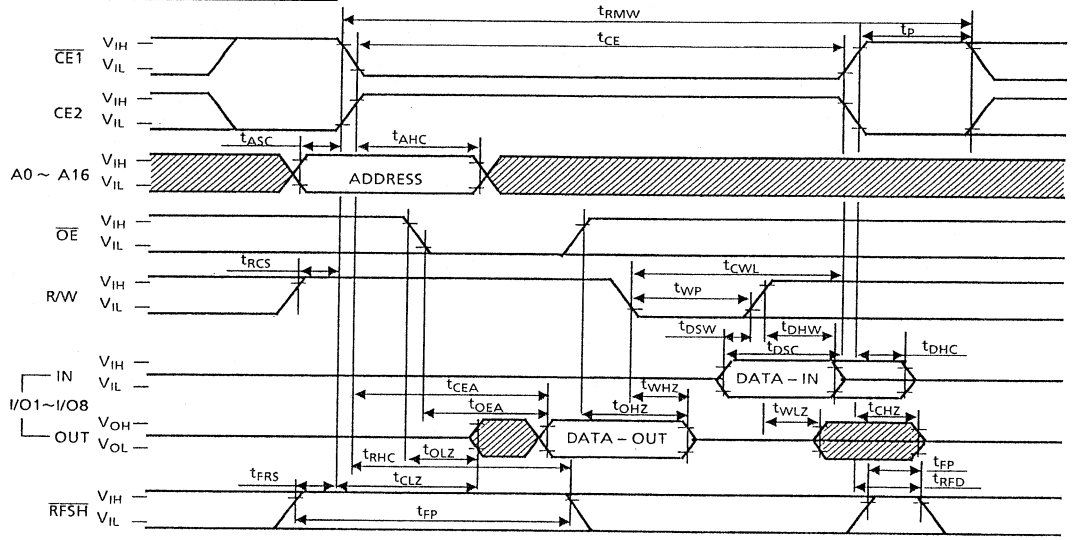


WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)

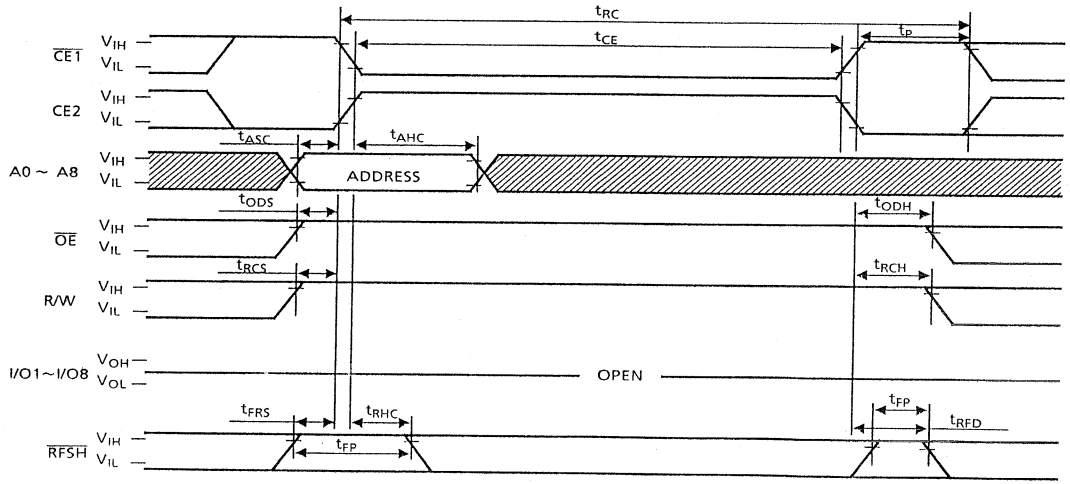


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

READ MODIFY WRITE CYCLE



CE ONLY REFRESH

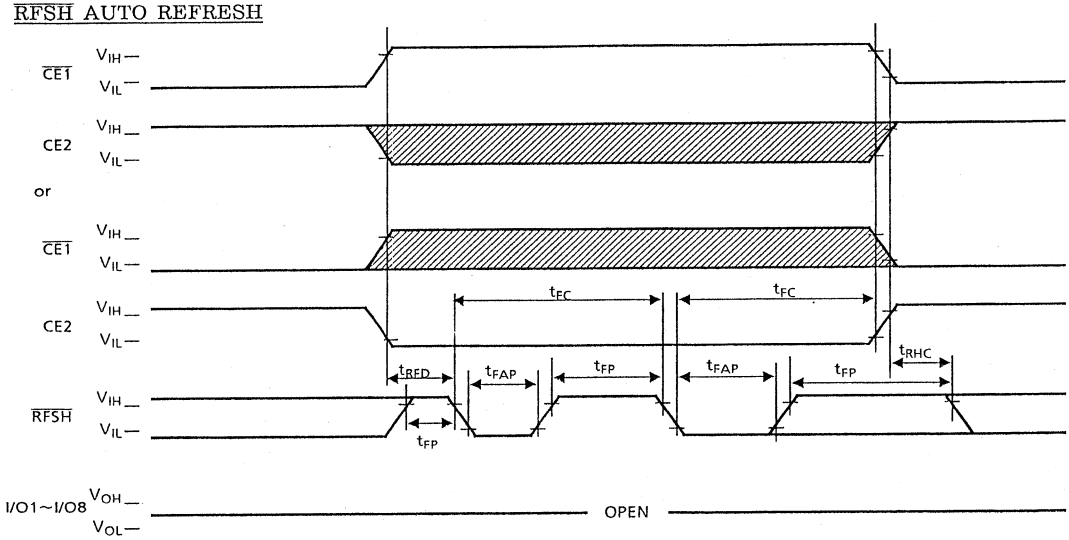


Note : A9 ~ A16 = Don't care

▨: Don't care

Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

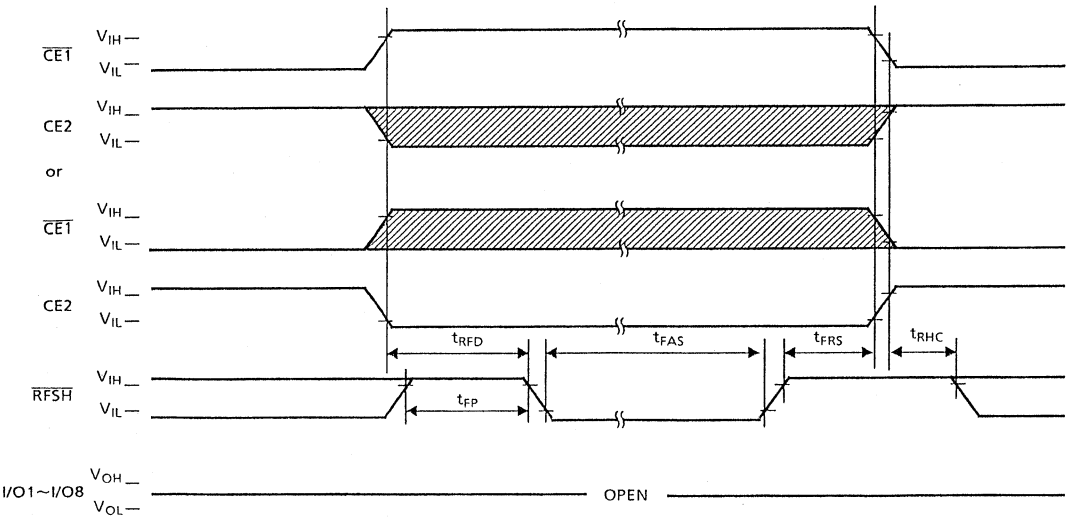
RFSH AUTO REFRESH



NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

SELF REFRESH



NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

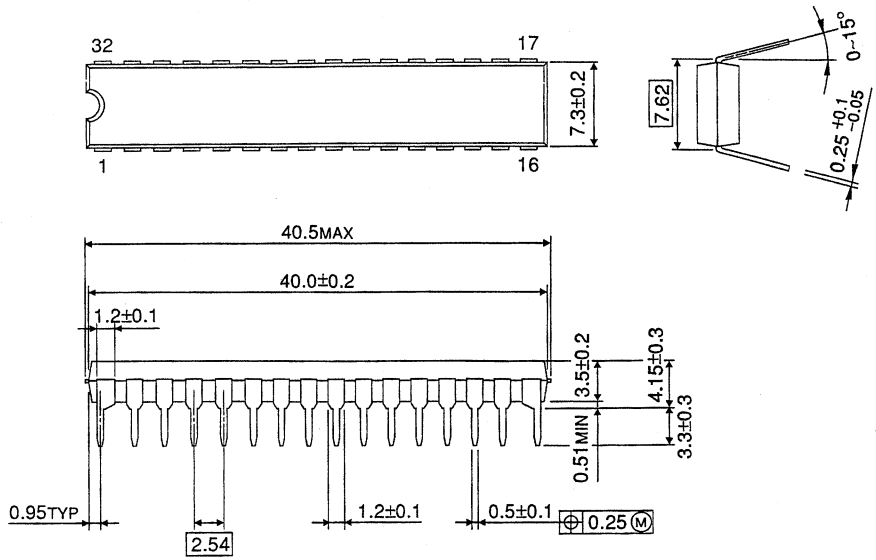
We hope this information will be very useful for you.

Nov. 1991

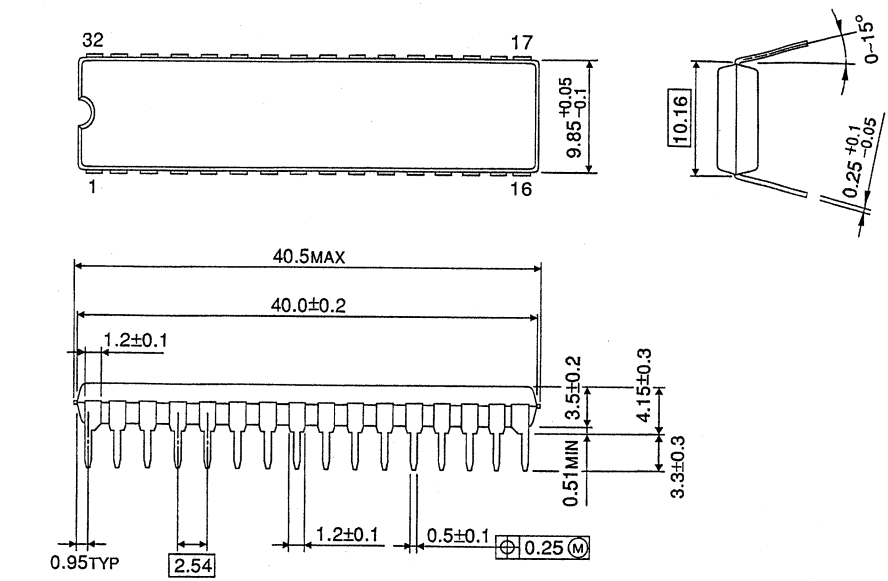
TOSHIBA CORPORATION
Semiconductor Group

Unit in mm

DIP32-P-300

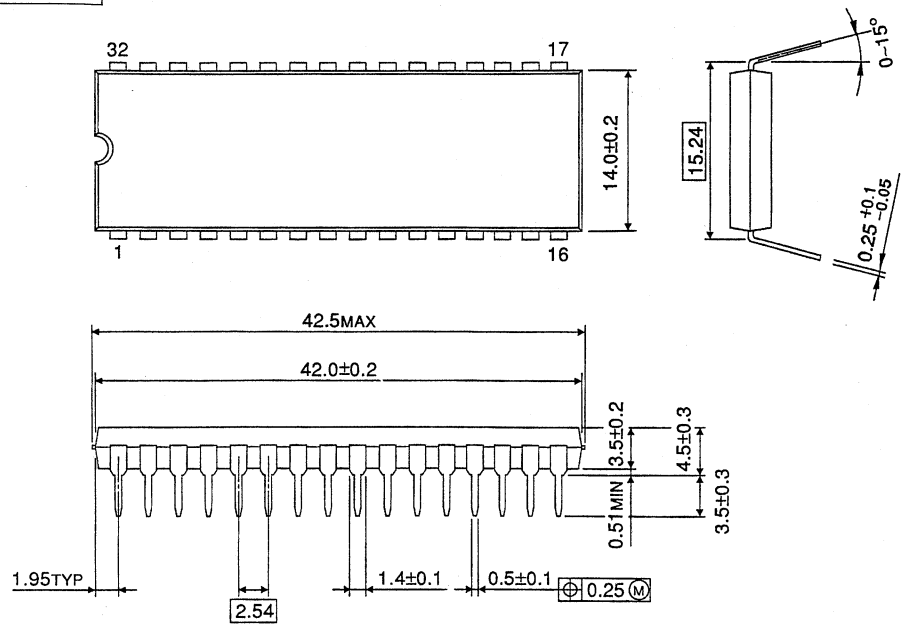


DIP32-P-400

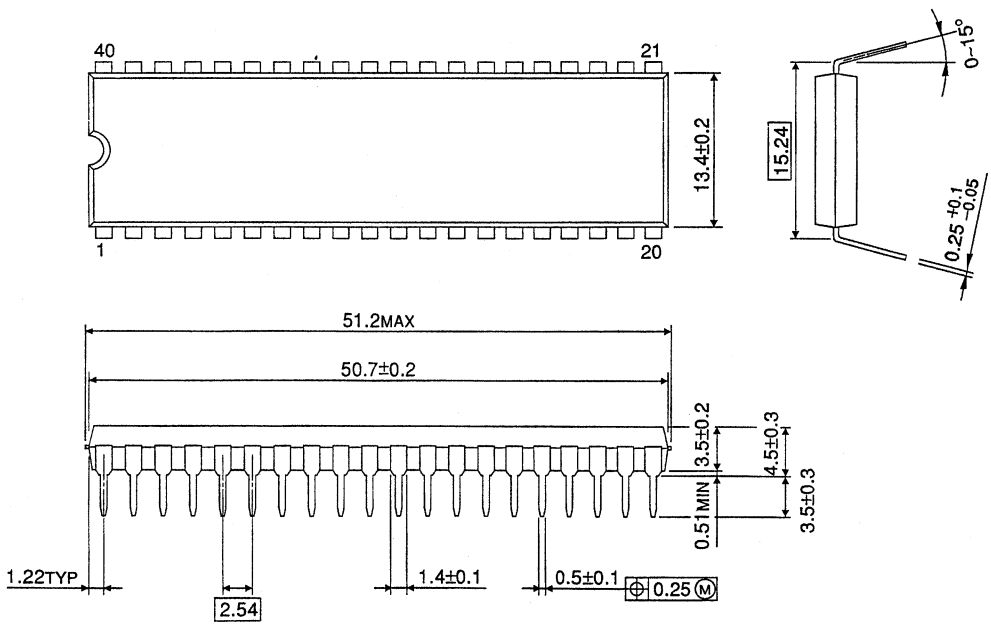


Unit in mm

DIP32-P-600

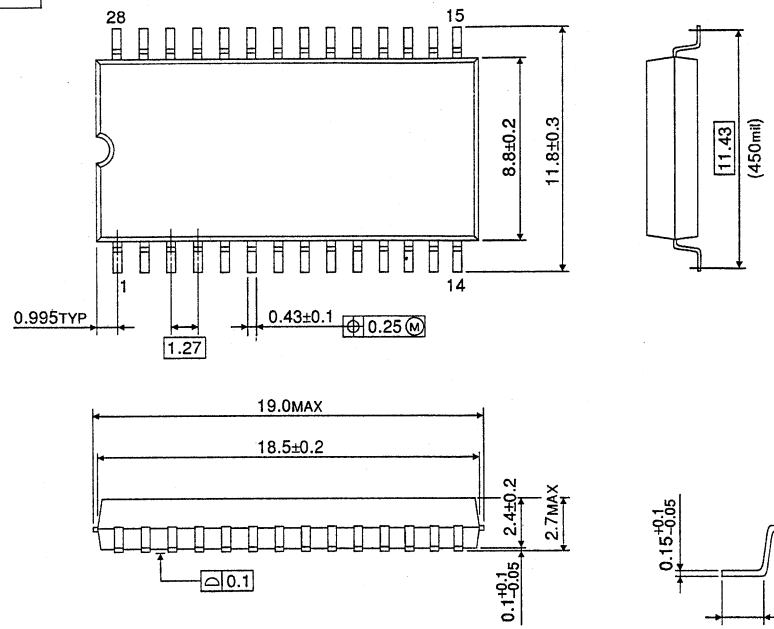


DIP40-P-600

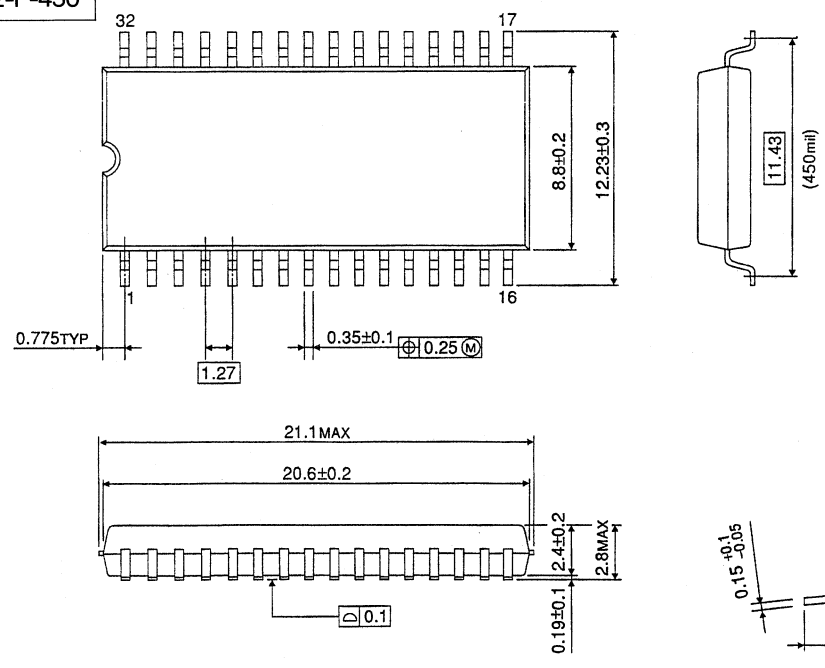


Unit in mm

SOP28-P-450

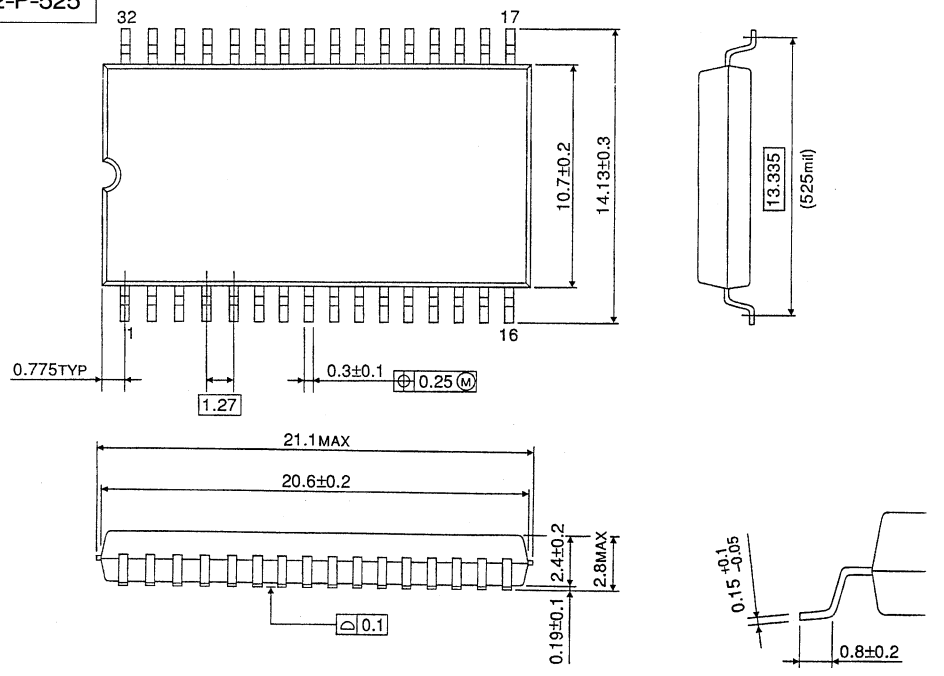


SOP32-P-450

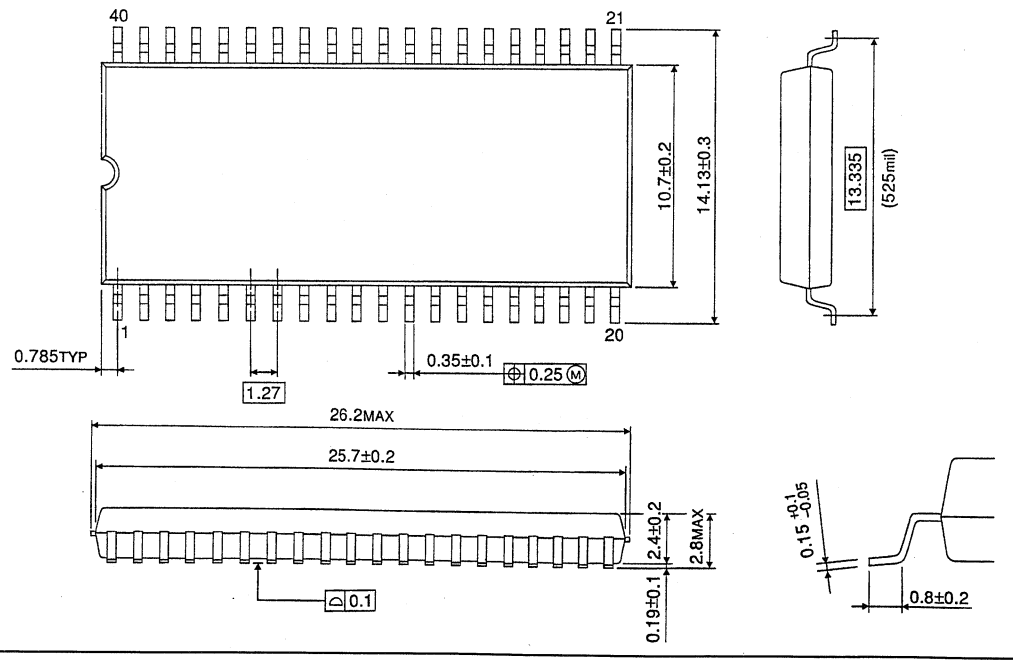


Unit in mm

SOP32-P-525



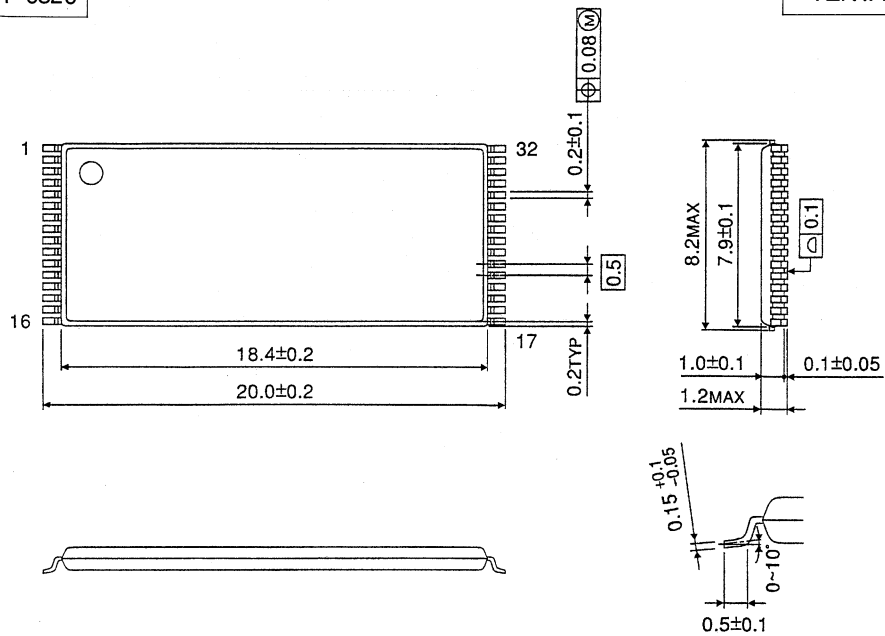
SOP40-P-525



Unit in mm

TSOP32-P-0820

TENTATIVE



TSOP32-P-0820A

TENTATIVE