

# TC518128APL/AFL/AFWL-80LV,-10LV,-12LV TC518128AFTL/ATRL-80LV,-10LV,-12LV

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

## DESCRIPTION

The TC518128A Family is a 1M bit high speed CMOS Pseudo Static RAM organized as 131,072 words by 8 bits. The TC518128A Family utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. The feature includes single power supply of 5V ± 10%. The RFSH input allows two types of refresh operation - auto refresh and self refresh. The TC518128A Family also features static RAM like write function that the input data is written into the memory cell at the rising edge of R/W, thus being easy to interface with microprocessor.

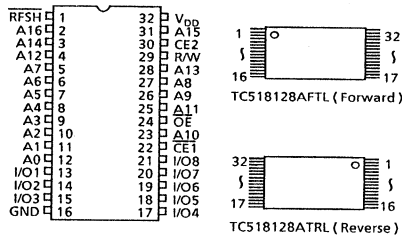
The TC518128A Family is a pin-compatible with 1M bit CMOS Static RAM - JEDEC standard and is moulded in a 32 pin standard 0.6 inch and 0.3 inch width plastic DIP and small - out line plastic flat package and a 32 pin plastic thin small - out - line package (forward, reverse type).

## FEATURES

- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation
- Single Power Supply : 5V ± 10%
- Data Retention Supply Voltage : 3.0V ~ 5.5V
- Auto refresh is capable by internal counter.
- Self refresh is capable by internal timer.
- All inputs and outputs : TTL compatible
- 512 refresh cycle/8ms
- Auto refresh power down function
- Pin Compatible : 1M SRAM (JEDEC)
- Logic Compatible : SRAM R/W Pin
- Logic Compatible : SRAM R/W Pin
- Package : TC518128APL : DIP32-P-600  
TC518128AFL : SOP32-P-450  
TC518128AFWL : SOP32-P-525  
TC518128AFTL : TSOP32-P-0820  
TC518128ATRL : TSOP32-P-0820A

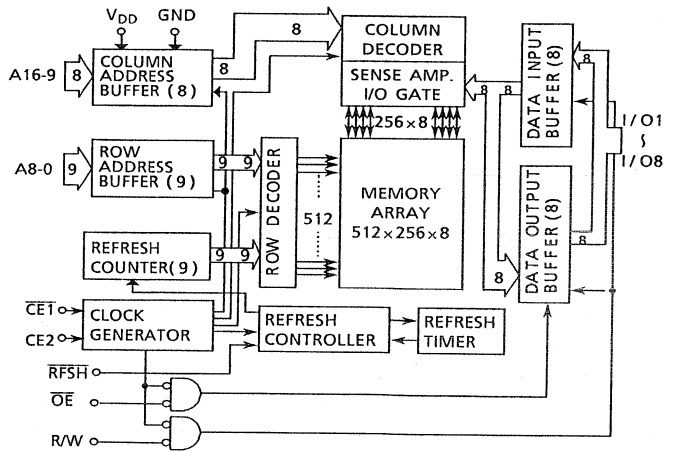
	TC518128A Family		
	- 80	- 10	- 12
t <sub>CEA</sub> CE Access Time	80ns	100ns	120ns
t <sub>OE</sub> OE Access Time	35ns	40ns	50ns
t <sub>rc</sub> Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	5.5V	200µA	
	3.0V	100µA	

## PIN CONNECTION (TOP VIEW)



TC518128APL / AFL / ASPL / AFWL

## BLOCK DIAGRAM



## PIN NAMES

A0~A16	Address Inputs
R/W	Read / Write Control Input
OE	Output Enable Input
RFSH	Refresh Input
CE1, CE2	Chip Enable Inputs
I/O1~I/O8	Data Inputs / Outputs
V <sub>DD</sub>	Power
GND	Ground

(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A <sub>11</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>13</sub>	R/W	CE2	A <sub>15</sub>	V <sub>DD</sub>	RFSH	A <sub>16</sub>	A <sub>14</sub>	A <sub>12</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE1	A <sub>10</sub>	OE

# TC518128APL/AFL/AFWL-80LV,-10LV,-12LV

## TC518128AFTL/ATRL-80LV,-10LV,-12LV

### FUNCTION LOGIC

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O ~ 8	CONDITION
L	H	L	H	*	V*	OUT	Read
L	H	*	L	*	V*	IN	Write
L	H	H	H	*	V*	HZ	CE only Refresh
H	*	*	*	L	*	HZ	Auto/Self Refresh
*	L	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by
*	L	*	*	H	*	HZ	Stand by

H ... High Level Input ( $V_{IN} = 6.5V \sim V_{IH}$  min. )

L ... Low Level Input ( $V_{IN} = V_{IL}$  max.  $\sim -1.0V$ )

\* ... Don't care ( $6.5V \sim -1.0V$ )

V\* ... At  $\overline{CE1}$  falling edge ( $CE2 = H$ ) or CE2 rising edge ( $\overline{CE1} = L$ ), all address inputs are "IN", and at the other condition, the address input are "\*".

HZ ... High Impedance

### ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
$V_{IN}$	Input Voltage	-1.0~7.0	V	1
$V_{OUT}$	Output Voltage	-1.0~7.0	V	
$V_{DD}$	Power Supply Voltage	-1.0~7.0	V	
$T_{OPR}$	Operating Temperature	0~70	°C	
$T_{STG}$	Storage Temperature	-55~150	°C	
$T_{SOLDER}$	Soldering Temperature · Time	260 · 10	°C · sec	
$P_D$	Power Dissipation	600	mW	
$I_{OUT}$	Short Circuit Output Current	50	mA	

### D.C. RECOMMENDED OPERATING CONDITIONS ( $T_a = 0 \sim 70^\circ C$ )

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
$V_{DD}$	Power Supply Voltage	4.5	5.0	5.5	V	2
$V_{IH}$	Input High Voltage	2.4	-	6.5	V	
$V_{IL}$	Input Low Voltage	-1.0	-	0.8	V	

# TC518128APL/AFL/AFWL-80LV,-10LV,-12LV TC518128AFTL/ATRL-80LV,-10LV,-12LV

## D.C. ELECTRICAL CHARACTERISTICS ( $V_{DD} = 5V \pm 10\%$ , $T_a = 0 \sim 70^\circ C$ )

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES	
$I_{DDO}$	Operating Current (Average Power Supply Operating Current) $\overline{CE1}$ , CE2, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	80ns version	-	50	70	mA	3, 4
		100ns version	-	40	60		
		120ns version	-	35	50		
$I_{DD51}$	Standby Current, $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ , $\overline{RFSH} = V_{IH}$	-	-	1	mA		
$I_{DD52}$	Standby Current, $\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$ , $\overline{RFSH} = V_{DD} - 0.2V$	-	100	200	$\mu A$		
$I_{DDF1}$	Self Refresh Current (Average Current), $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ , $\overline{RFSH} = V_{IL}$	-	-	1	mA		
$I_{DDF2}$	Self Refresh Current (Average Current) $\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$ , $\overline{RFSH} = V_{IL}$	-	100	200	$\mu A$		
$I_{DDF3}$	Auto Refresh Current (Average Current) ( $\overline{RFSH}$ cycling : $t_{FC} = t_{FC \text{ min}}$ )	-	-	2	mA		
$I_{DDF4}$	CE only Refresh Current (Average Current) ( $\overline{CE1}$ , CE2, Address cycling : $t_{RC} = t_{RC \text{ min}}$ )	80ns version	-	50	70	mA	3
		100ns version	-	40	60		
		120ns version	-	35	50		
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$ , All other Inputs not under test = 0V	-10	-	10	$\mu A$		
$I_{O(L)}$	Output Leakage Current Output Disable ( $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$ ), $0V \leq V_{OUT} \leq V_{DD}$	-10	-	10	$\mu A$		
$V_{OH}$	Output High Level $I_{OH} = -5mA$	2.4	-	-	V		
$V_{OL}$	Output Low Level $I_{OL} = 4.2mA$	-	-	0.4	V		

Note) In  $I_{DD51}$  and  $I_{DDF1}$  with  $\overline{CE1} = V_{IH}$  ( $CE2 = V_{IL}$ ), these specification limits are guaranteed under the condition of  $CE2 = V_{IH}$  or  $CE2 = V_{IL}$  ( $\overline{CE1} = V_{IH}$  or  $\overline{CE1} = V_{IL}$ ). In  $I_{DD52}$  and  $I_{DDF2}$  with  $\overline{CE1} \geq V_{DD} - 0.2V$  ( $CE2 \leq 0.2V$ ), these specification are guaranteed under the condition of  $CE2 \geq V_{DD} - 0.2V$  or  $CE2 \leq 0.2V$  ( $\overline{CE1} \geq V_{DD} - 0.2V$  or  $\overline{CE1} \leq 0.2V$ ).

## CAPACITANCE ( $V_{DD} = 5V$ , $f = 1MHz$ , $T_a = 25^\circ C$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$C_{I1}$	Input Capacitance (A0 ~ A16)	-	5	pF
$C_{I2}$	Input Capacitance ( $\overline{CE1}$ , CE2, $\overline{OE}$ , R/W, $\overline{RFSH}$ )	-	7	pF
$C_{I0}$	Input/Output Capacitance	-	7	pF

Note) This parameter periodically sampled is not 100% tested.

# TC518128APL/AFL/AFWL-80LV,-10LV,-12LV TC518128AFTL/ATRL-80LV,-10LV,-12LV

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

( $V_{DD} = 5V \pm 10\%$ ,  $T_a = 0 \sim 70^\circ C$ ) (NOTES: 5, 6, 7, 8)

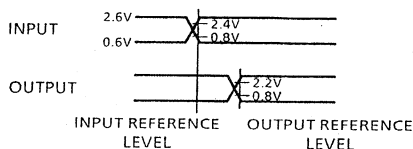
SYMBOL	PARAMETER	- 80		- 10		- 12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{RC}$	Random Read, Write Cycle Time	130	-	160	-	190	-	ns	
$t_{RMW}$	Read Modify Write Cycle Time	195	-	235	-	280	-	ns	
$t_{CE}$	CE Pulse Width	80	10,000	100	10,000	120	10,000	ns	13
$t_P$	CE Precharge Time	40	-	50	-	60	-	ns	
$t_{CEA}$	CE Access Time	-	80	-	100	-	120	ns	
$t_{OEA}$	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
$t_{CLZ}$	CE to Output in Low-Z	30	-	30	-	30	-	ns	
$t_{OLZ}$	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
$t_{WLZ}$	Output Active from End of Write	0	-	0	-	0	-	ns	
$t_{CHZ}$	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
$t_{OHZ}$	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
$t_{WHZ}$	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
$t_{ODS}$	$\overline{OE}$ Output Disable Set-Up Time	0	-	0	-	0	-	ns	
$t_{ODH}$	$\overline{OE}$ Output Disable Hold Time	10	-	10	-	10	-	ns	
$t_{RCS}$	Read Command Set-Up Time	0	-	0	-	0	-	ns	
$t_{RCH}$	Read Command Hold Time	0	-	0	-	0	-	ns	
$t_{Wp}$	Write Pulse Width	60	-	70	-	85	-	ns	
$t_{WCH}$	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
$t_{CWL}$	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000	ns	
$t_{DSW}$	Data Set-Up Time from R/W	30	-	35	-	45	-	ns	10
$t_{DSC}$	Data Set-Up Time from CE	30	-	35	-	45	-	ns	10
$t_{DHW}$	Data Hold Time from R/W	0	-	0	-	0	-	ns	10
$t_{DHC}$	Data Hold Time from CE	0	-	0	-	0	-	ns	10
$t_{ASC}$	Address Set-Up Time	0	-	0	-	0	-	ns	11
$t_{AHC}$	Address Hold Time	20	-	25	-	30	-	ns	11
$t_{RHC}$	$\overline{RFSH}$ Command Hold Time	15	-	15	-	15	-	ns	
$t_{FC}$	Auto Refresh Cycle Time	130	-	160	-	190	-	ns	
$t_{RFD}$	$\overline{RFSH}$ Delay Time from CE	40	-	50	-	60	-	ns	
$t_{FAP}$	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
$t_{FP}$	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	12
$t_{FAS}$	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	8,000	-	8,000	-	ns	12
$t_{FRS}$	CE Delay Time from $\overline{RFSH}$ (Self Refresh)	160	-	190	-	225	-	ns	12
$t_{REF}$	Refresh Period (512 cycle, A0~A8)	-	8	-	8	-	8	ms	
$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
$t_{CES}$	CE2 Low Set - Up Time	5	-	5	-	5	-	ns	14
$t_{CEH}$	CE2 Low Hold Time	5	-	5	-	5	-	ns	14

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**NOTES :**

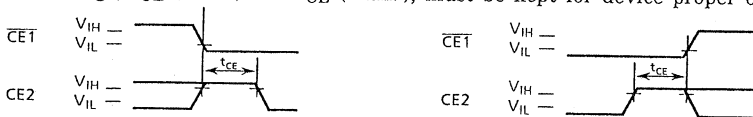
- 1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- 2) All voltage are referenced to GND.
- 3)  $I_{DDO}$  and  $I_{DDF4}$  depends on cycle rate.
- 4)  $I_{DDO}$  depends on output loading. Specified values are obtained with the output open.
- 5) An initial pause of  $100\mu s$  with high  $\overline{CE1}$  or low CE2 is required after power-up, before proper device operation is achieved.
- 6) AC measurements assume  $t_T = 5ns$ .
- 7) Timing reference level

Input Level :  $V_{IH} = 2.6V$   
 $V_{IL} = 0.6V$   
 Input Reference Level :  $V_{IH} = 2.4V$   
 $V_{IL} = 0.8V$   
 Output Reference Level:  $V_{OH} = 2.2V$   
 $V_{OL} = 0.8V$

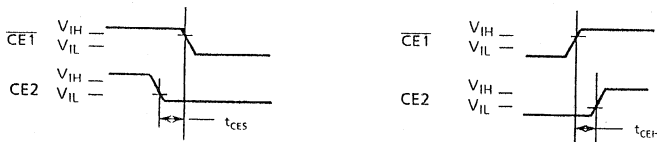


- 8) Measured with a load equivalent to 2 TTL loads and  $100pF$ .
- 9)  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) In write cycles, the input data is latched at the earlier of R/W or  $\overline{CE1}$  rising edge and CE2 falling edge. Therefore the input data must be valid during set-up time ( $t_{DSW}$  or  $t_{DSC}$ ) and hold time ( $t_{DHW}$  or  $t_{DHC}$ ).
- 11) All address inputs are latched at the falling edge of  $\overline{CE1}$  and the rising edge of CE2. Therefore the all address inputs must be valid during  $t_{ASC}$  and  $t_{AHC}$ .
- 12) Two refresh operation - auto refresh and self refresh are defined by the  $\overline{RFSH}$  pulse width under the condition of  $\overline{CE1} = V_{IH}$  or  $CE2 = V_{IL}$ .  
 Auto refresh :  $\overline{RFSH}$  pulse width  $\leq t_{FAP}(\max.)$   
 Self refresh :  $\overline{RFSH}$  pulse width  $\geq t_{FAS}(\min.)$   
 The timing parameter ( $t_{FRS}$ ) must be kept for device proper operation in the following conditions.
  - after self refresh
  - in case of  $\overline{RFSH} = "L"$  after power-up

- 13) The timings,  $t_{CE}(\min.)$  and  $t_{CE}(\max.)$ , must be kept for device proper operation as follows.



- 14) The timings,  $t_{CES}(\min.)$  and  $t_{CEH}(\min.)$ , must be kept for using  $\overline{CE1}$  and CE2 at the same clock as follow.



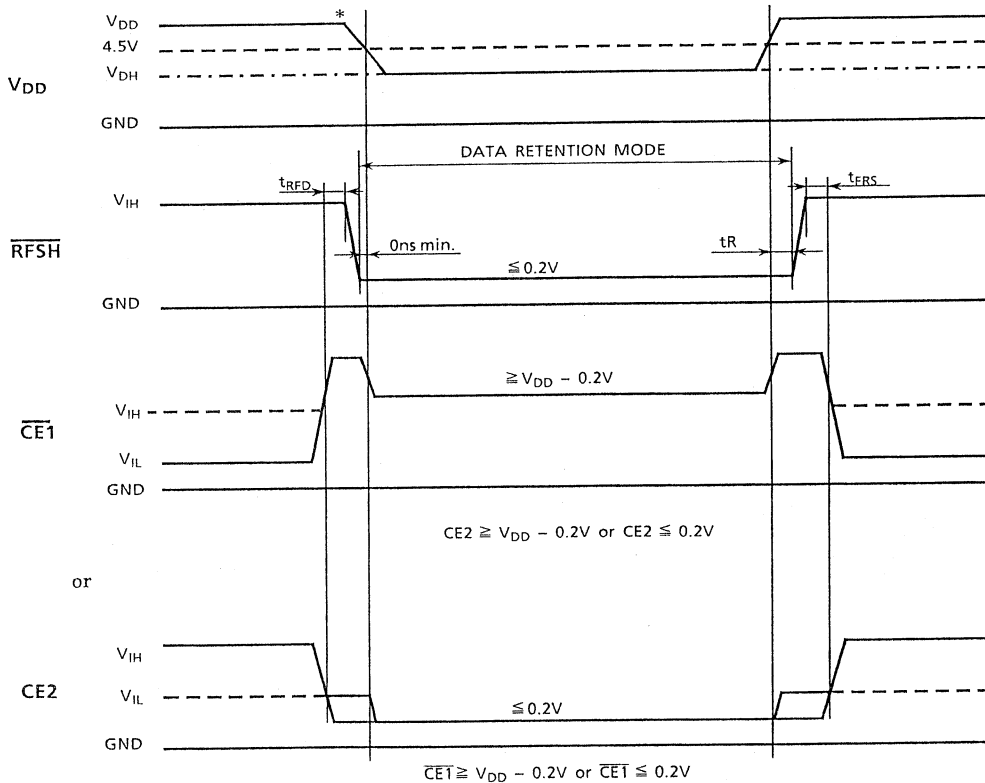
# TC518128APL/AFL/AFWL-80LV,-10LV,-12LV

## TC518128AFTL/ATRL-80LV,-10LV,-12LV

### DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	
V <sub>DH</sub>	Data Retention Supply Voltage	3.0	-	5.5	V	
I <sub>DDF2</sub>	Self Refresh Current	V <sub>DH</sub> = 3.0V	-	40	100	μA
		V <sub>DH</sub> = 5.5V	-	100	200	μA
t <sub>R</sub>	Recovery Time	5	-	-	mS	

\*The falling slope of V<sub>DD</sub> must be more than 50ms in order to operate the device safely. (20ms/V)



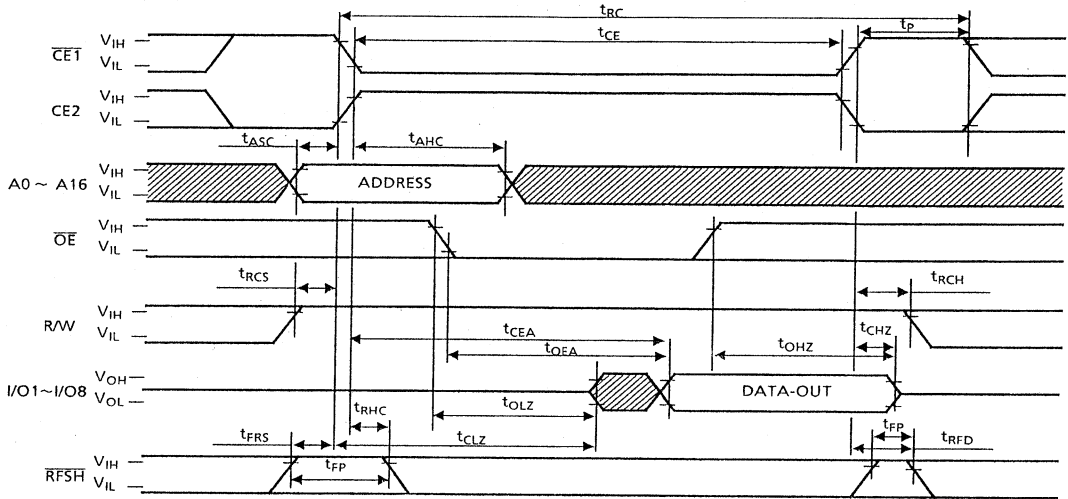
(Note) °  $\overline{OE}$ , R/W, A0~A16 = Don't care

- ° I<sub>DDF1</sub> is applied in  $\overline{RFSH} = V_{IL \text{ max.}}$ ,  $\overline{CE1} = V_{IH \text{ min.}}$ ,  $CE2 = V_{IL \text{ max.}}$ .
- ° At any state but Data Retention Mode, Auto Refresh or CE Only Refresh with 512cycle/8ms is required.

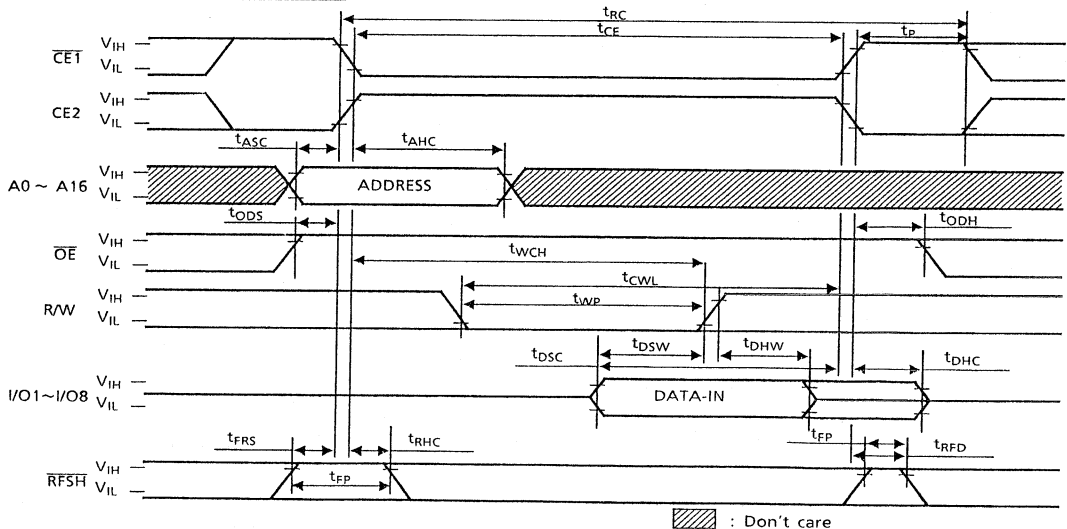
# TC518128 APL/AFL/AFWL-80LV,-10LV,-12LV TC518128 AFTL/ATRL-80LV,-10LV,-12LV

## TIMING WAVEFORMS

### READ CYCLE



### WRITE CYCLE-1 ( $\overline{OE}$ Fix High)



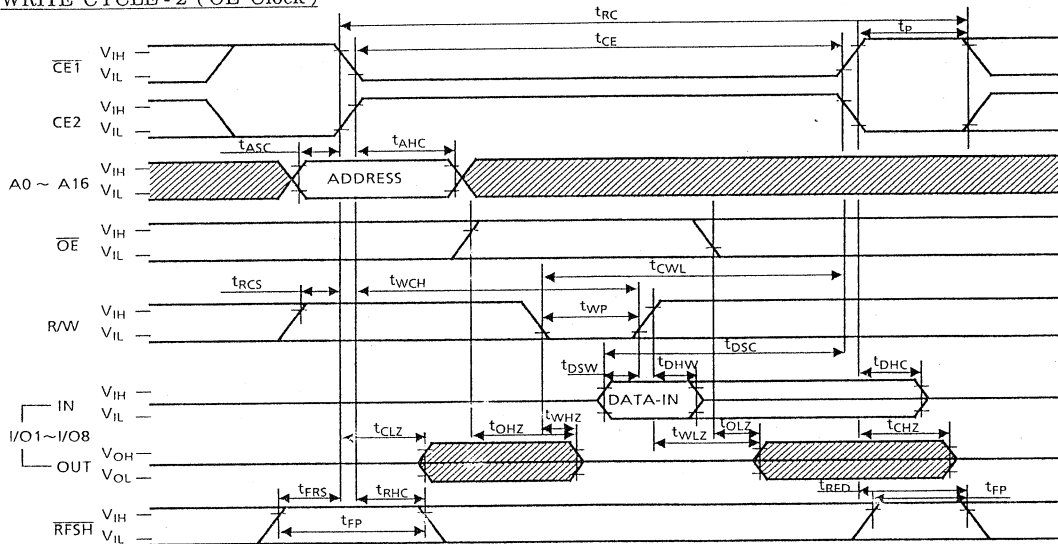
▨ : Don't care

Note: The device can be operated with cycling " $\overline{CE1}$ " (or CE2) pin only, provided that " $\overline{CE2}$ " (or " $\overline{CE1}$ ") is connected to  $V_{IH}$  (or  $V_{IL}$ ) level.

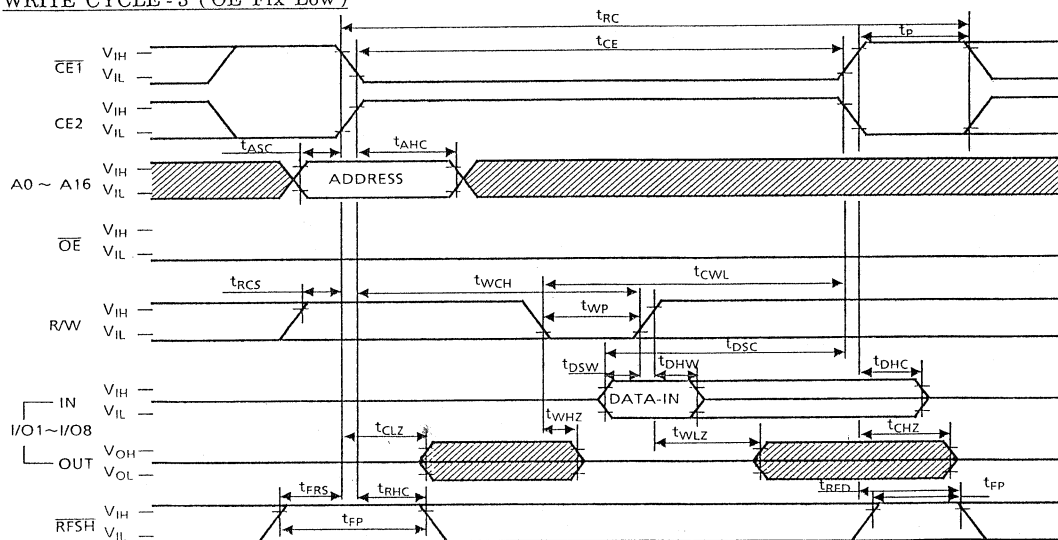
# TC518128APL/AFL/AFWL-80LV,-10LV,-12LV

## TC518128AFTL/ATRL-80LV,-10LV,-12LV

WRITE CYCLE - 2 ( $\overline{OE}$  Clock)



WRITE CYCLE - 3 ( $\overline{OE}$  Fix Low)



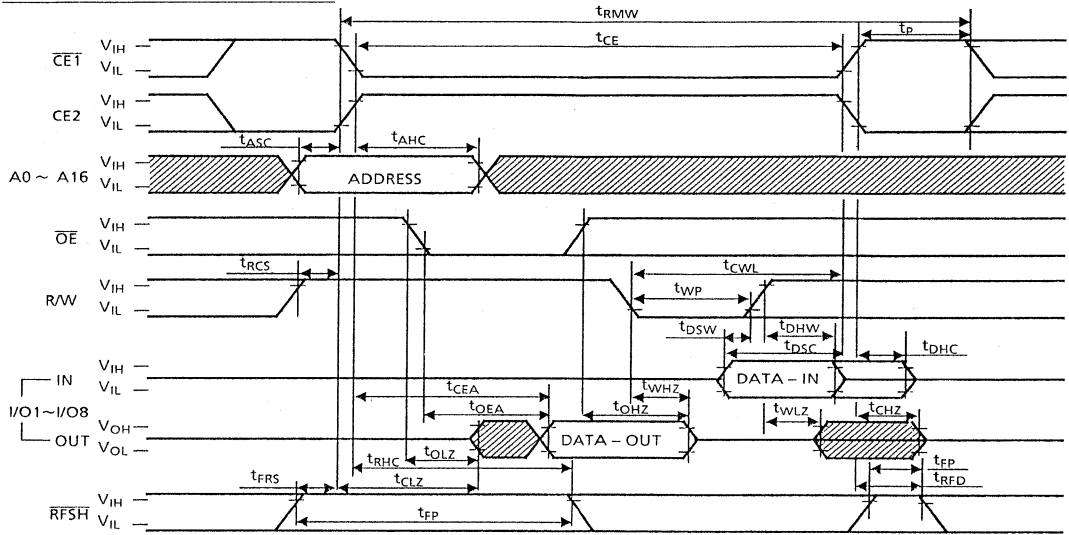
▨ : Don't care

Note: The device can be operated with cycling " $\overline{CE1}$ " (or  $CE2$ ) pin only, provided that " $CE2$ " (or " $\overline{CE1}$ ") is connected to  $V_{IH}$  (or  $V_{IL}$ ) level.

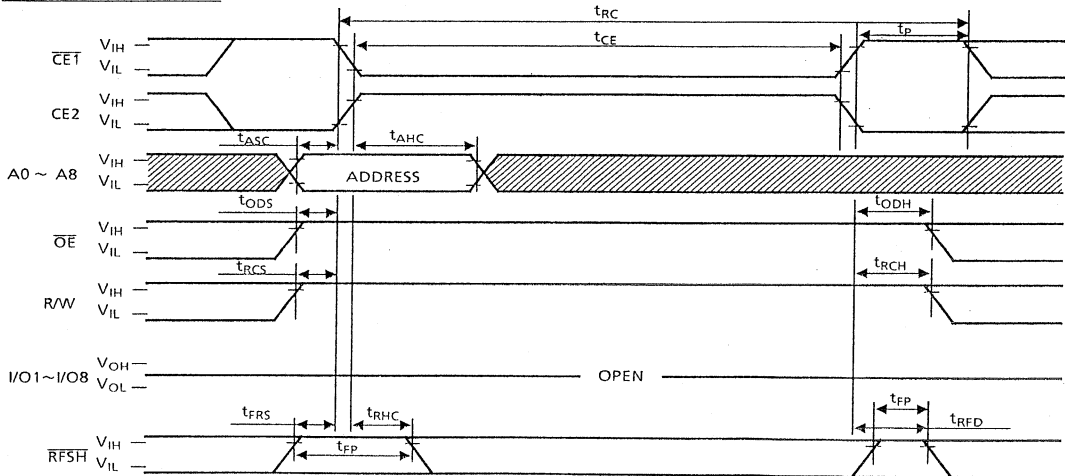


# TC518128APL/AFL/AFWL-80LV,-10LV,-12LV TC518128AFTL/ATRL-80LV,-10LV,-12LV

## READ MODIFY WRITE CYCLE



## CE ONLY REFRESH



Note : A9~A16 = Don't care

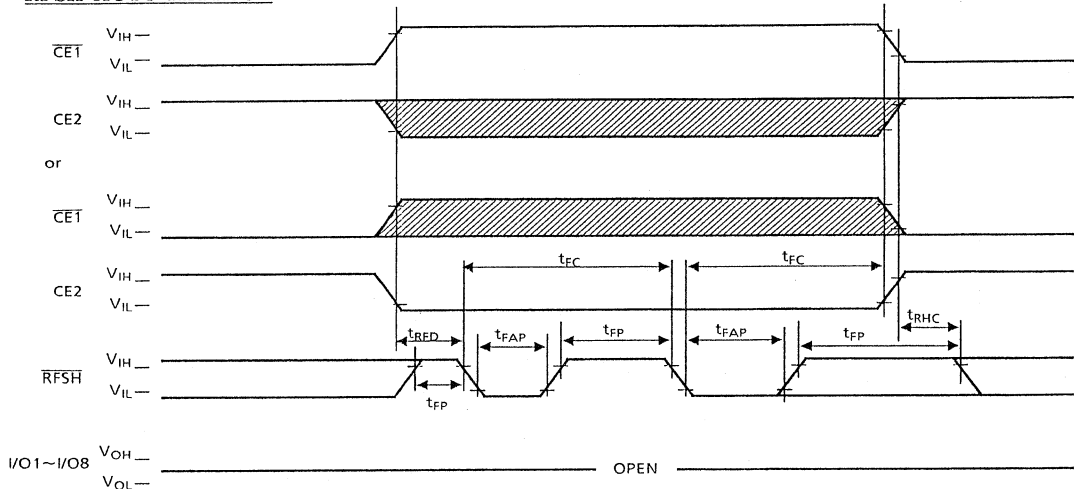
▨ : Don't care

Note: The device can be operated with cycling "CE1" (or CE2) pin only, provided that "CE2" (or "CE1") is connected to  $V_{IH}$  (or  $V_{IL}$ ) level.

# TC518128APL/AFL/AFWL-80LV,-10LV,-12LV

## TC518128AFTL/ATRL-80LV,-10LV,-12LV

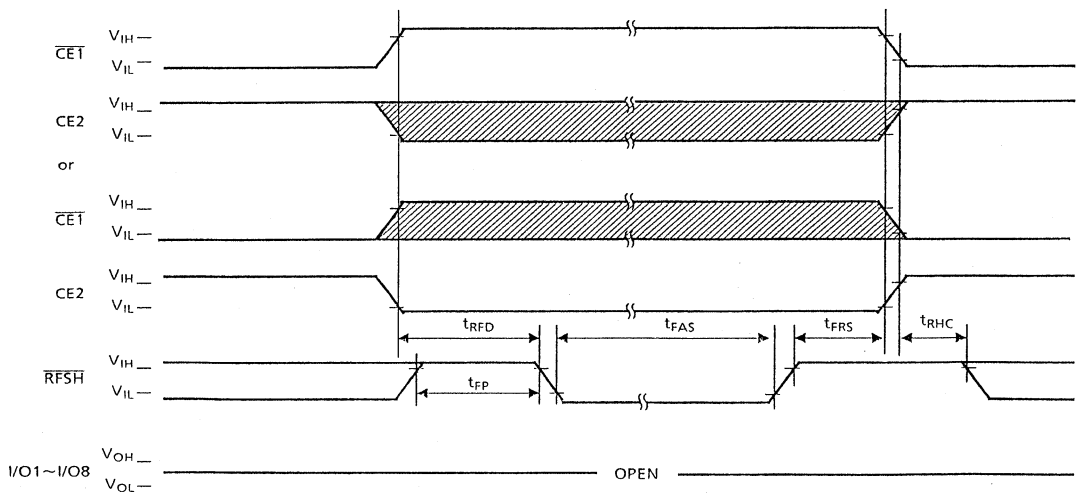
### RFSH AUTO REFRESH



NOTE :  $\overline{OE}$ , R/W, A0~A16 = Don't care

: Don't care

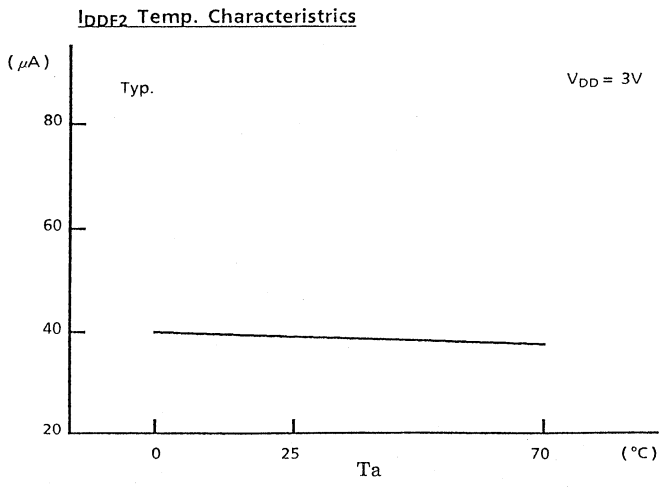
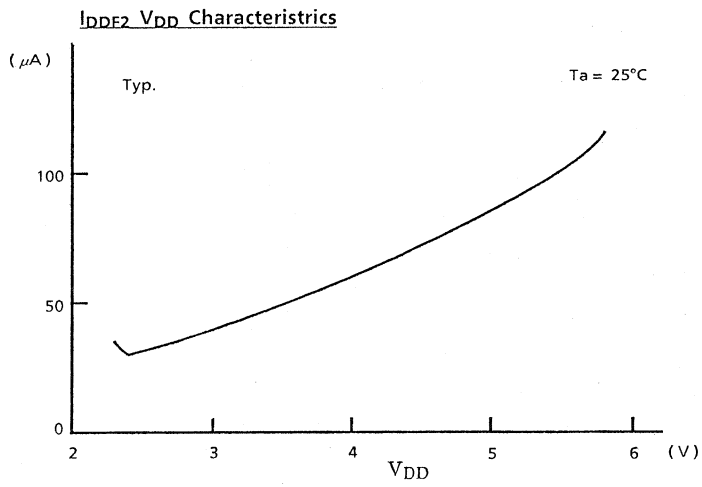
### SELF REFRESH



NOTE :  $\overline{OE}$ , R/W, A0~A16 = Don't care

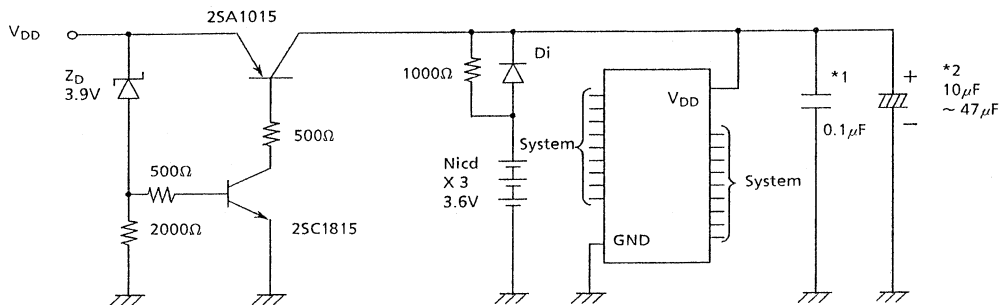
: Don't care

**TC518128APL/AFL/AFWL-80LV,-10LV,-12LV**  
**TC518128AFTL/ATRL-80LV,-10LV,-12LV**



# TC518128 APL/AFL/AFWL-80LV,-10LV,-12LV TC518128 AFL/ATL-80LV,-10LV,-12LV

## Battery Back Up applicable example



\*1: Ceramic condenser

\*2: Tantalum condenser

(The large Bypass condenser is preferable, as the noise is absorbed when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turning-off of the power supply must be avoided. Enter the Self Refresh Mode before changing to Battery Back Up Power Supply.

**TOSHIBA**

DATA BOOK

**MOS MEMORY**  
(VRAM, SRAM)

**1991**

# INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

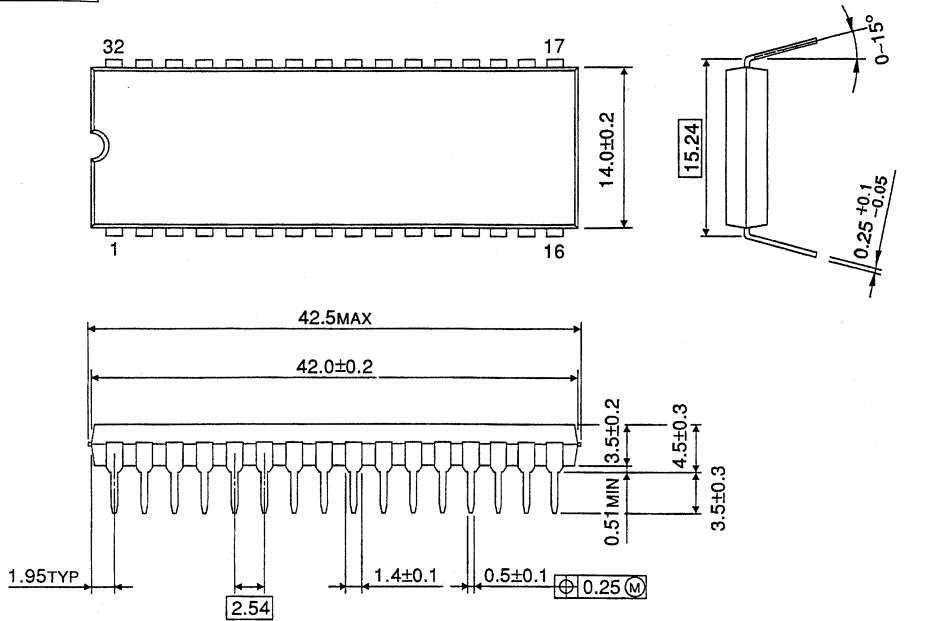
These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

We hope this information will be very useful for you.

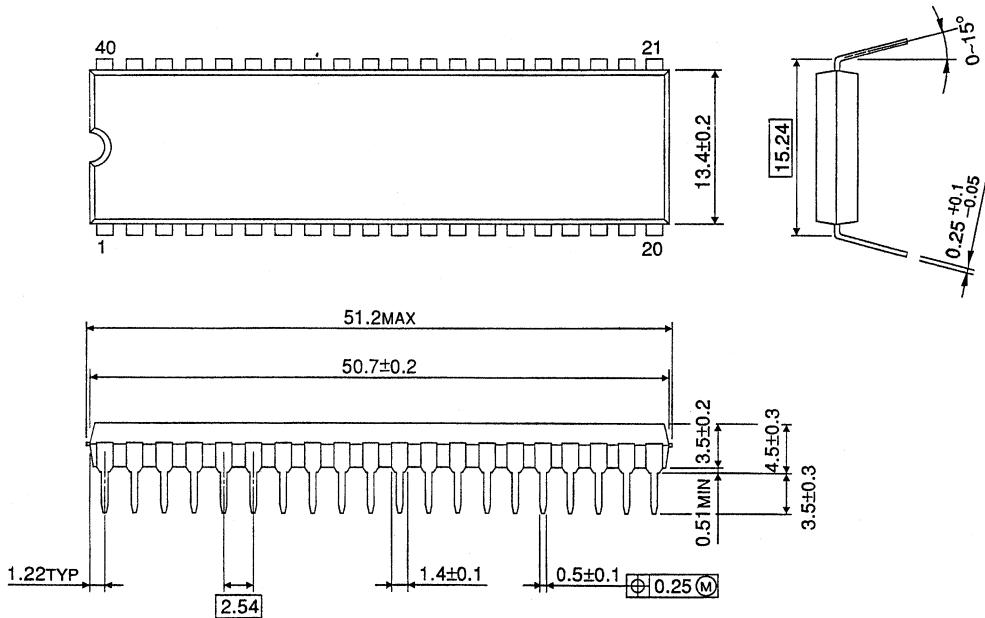
Nov. 1991

TOSHIBA CORPORATION  
Semiconductor Group

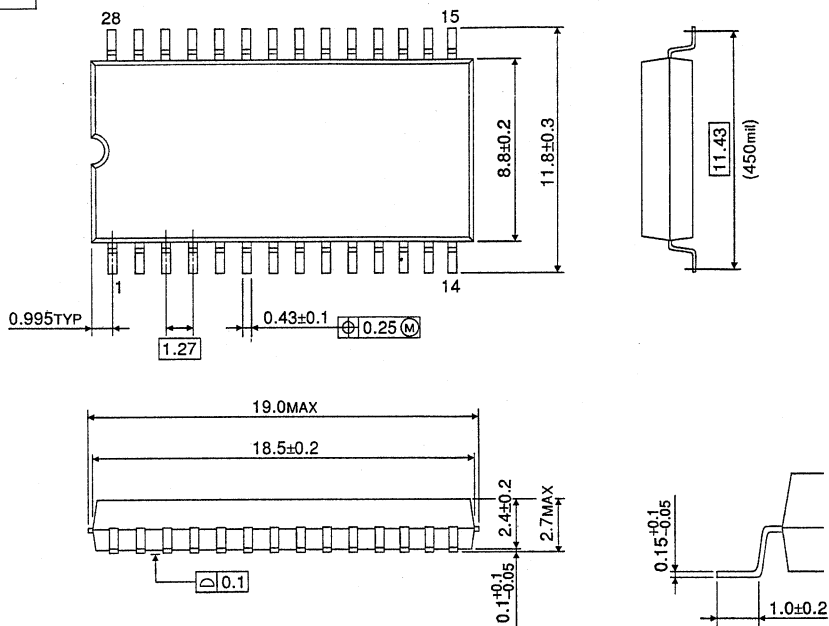
DIP32-P-600



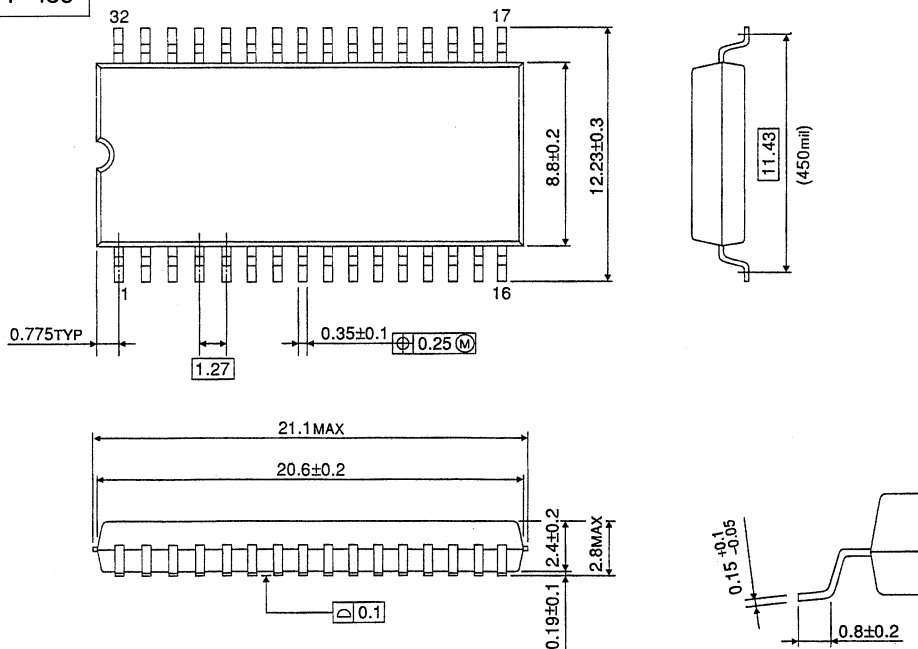
DIP40-P-600



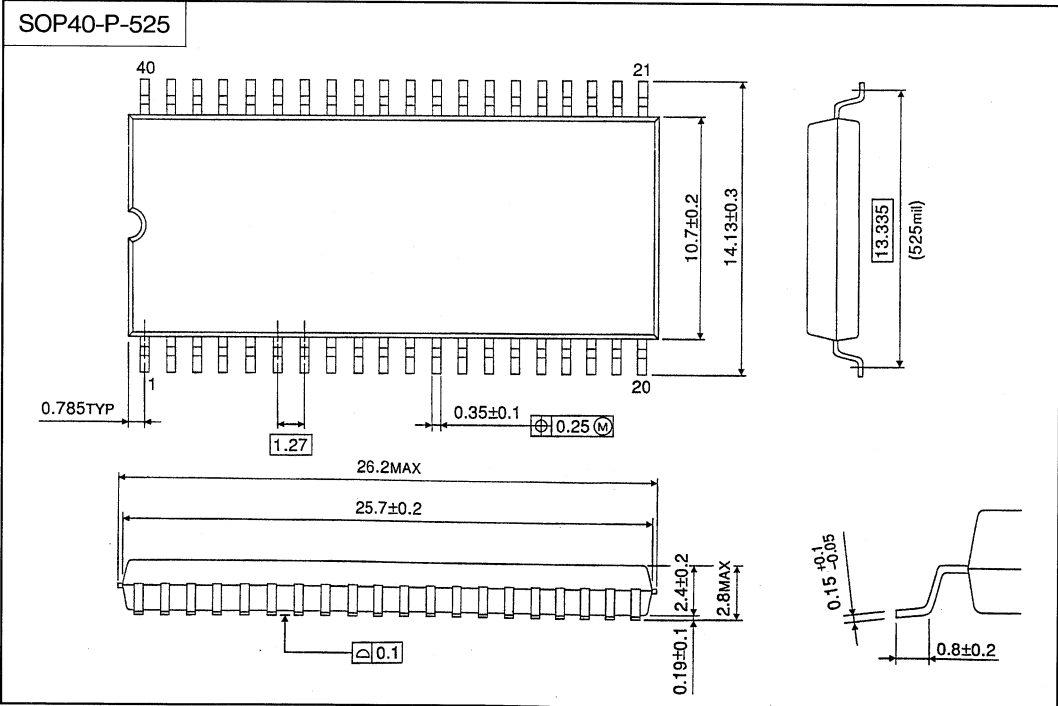
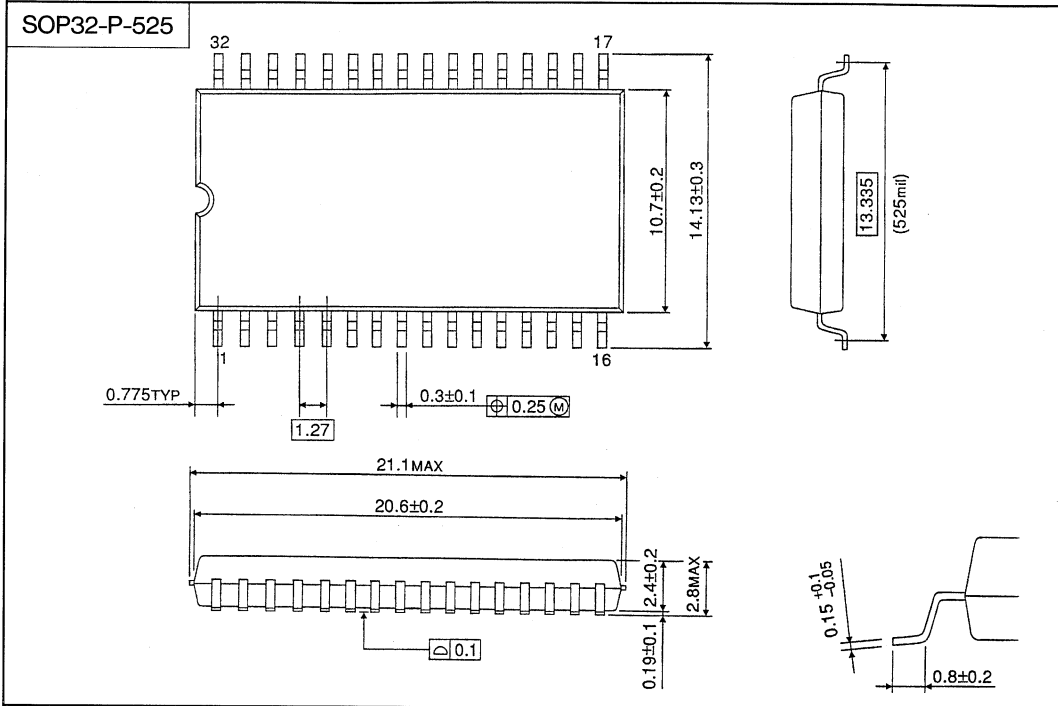
SOP28-P-450



SOP32-P-450

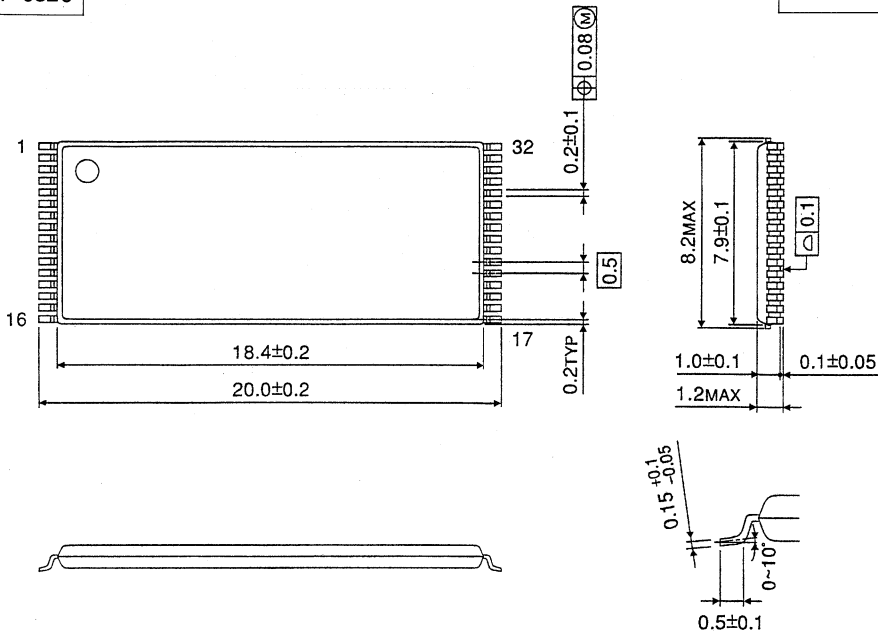






TSOP32-P-0820

TENTATIVE



TSOP32-P-0820A

TENTATIVE

