TC518512PL/FL-70,-80,-10
TC518512FTL/TRL-70,-80,-10

TENTATIVE DATA

524,288 WORDS × 8 BIT CMOS PSEUDO STATIC RAM TENTATIVE DATA

DESCRIPTION

The TC518512PL Family is a 4M bit high speed CMOS Pseudo Static RAM organized as 524,288 words by 8 bits. The TC518512PL Family utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. The feature includes single power supply of 5V±10%. The $\overline{OE}/\overline{RFSH}$ input allows two types of refresh operation - auto refresh and self refresh. The TC518512PL Family also features static RAM like write function that the input data is written into the memory cell at the rising edge of R/W, thus being easy to interface with microprocessor.

The TC518512PL Family is moulded in a 32 pin standard 0.6 inch width plastic DIP, Small Out line plastic flat Package and Thin Small Outline Package.

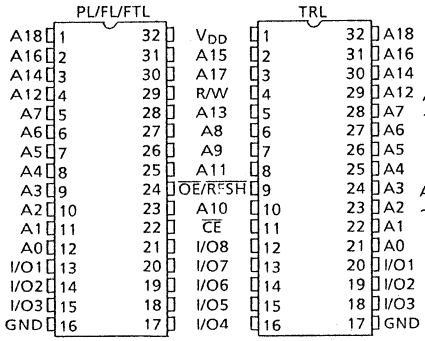
FEATURES

- Organization: 4M bit (524,288 word × 8bit)
- Fast Access Time and Low Power Dissipation

	TC518512PL Family		
	-70	-80	-10
t_{CEA} $\overline{CE}$ Access Time	70ns	80ns	100ns
t_{OEA} $\overline{OE}$ Access Time	30ns	30ns	40ns
t_{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	200μA		

- Single Power Supply : 5V±10%
- Auto refresh is capable by internal counter.
- Self refresh is capable by internal timer.
- All inputs and outputs : TTL compatible
- 2048 refresh cycle/32ms
- Logic Compatible: SRAM R/W Pin
- Package : TC518512PL : DIP32-P-600
  : TC518512FL : SOP32-P-525
  : TC518512FTL : TSOP32-P-400
  : TC518512TRL : TSOP32-P-400A

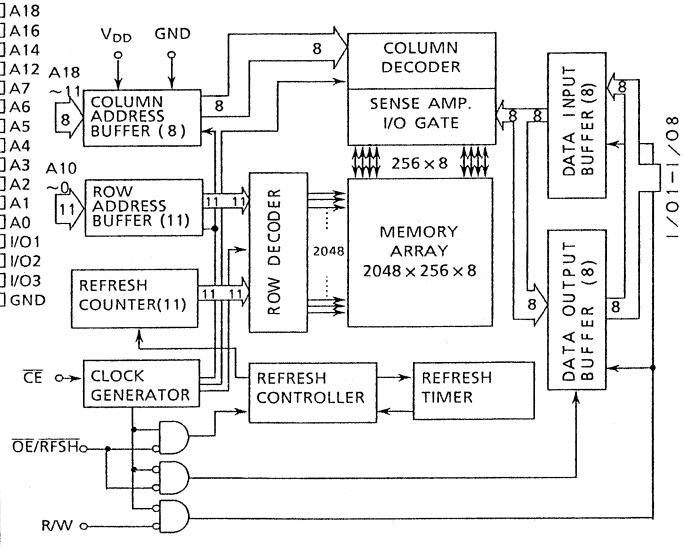
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A18	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable Input Refresh Input
$\overline{CE}$	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE}$	$\overline{OE}/\overline{RFSH}$	R/W	A0 ~ A18	I/O1 ~ 8	CONDITION
L	L	H	V*	OUT	Read
L	*	L	V*	IN	Write
L	H	H	V*	HZ	$\overline{CE}$ only Refresh
H	L	*	*	HZ	Auto/Self Refresh
H	H	*	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE}$ falling edge, all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}	Input Voltage	− 1.0~7.0	V	1
V_{OUT}	Output Voltage	− 1.0~7.0	V	
V_{DD}	Power Supply Voltage	− 1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	− 55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	− 1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTE
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	70ns version	–	50	70	mA	3, 4
		80ns version	–	45	60		
		100ns version	–	35	50		
I_{DDS1}	Standby Current $\overline{CE}$ = V_{IH}, $\overline{OE/RFSH}$ = V_{IH}		–	–	1	mA	
I_{DDS2}	Standby Current $\overline{CE}$ = V_{DD} – 0.2V, $\overline{OE/RFSH}$ = V_{DD} – 0.2V		–	–	200	μA	
I_{DDF1}	Self Refresh Current (Average Current) $\overline{CE}$ = V_{IH}, $\overline{OE/RFSH}$ = V_{IL}		–	–	1	mA	
I_{DDF2}	Self Refresh Current (Average Current) $\overline{CE}$ = V_{DD} – 0.2V, $\overline{OE/RFSH}$ = 0.2V		–	100	200	μA	
I_{DDF3}	Auto Refresh Current (Average Current) ($\overline{OE/RFSH}$ cycling : tFC = tFC min)		–	–	2	mA	
I_{DDF4}	$\overline{CE}$ only Refresh Current (Average Current) ($\overline{CE}$, Address cycling : tRC = tRC min)	70ns version	–	–	70	mA	3
		80ns version	–	–	60		
		100ns version	–	–	50		
$I_{I(L)}$	Input Leakage Current 0V ≦ V_{IN} ≦ V_{DD}, All other Inputs not under test = 0V		– 10	–	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE}$ = V_{IH} or $\overline{OE/RFSH}$ = V_{IH} or R/W = V_{IL}), 0V ≦ V_{OUT} ≦ V_{DD}		– 10	–	10	μA	
V_{OH}	Output High Level I_{OH} = – 1.0mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 2.1mA		–	–	0.4	V	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25 °C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A18)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{OE/RFSH}$, R/W)	–	7	pF
C_{IO}	Input / Output Capacitance	–	7	pF

Note) This parameter periodically sampled is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

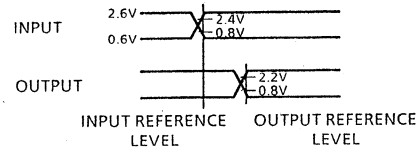
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	115	–	130	–	160	–	ns	
t_{RMW}	Read Modify Write Cycle Time	165	–	180	–	220	–	ns	
t_{CE}	$\overline{CE}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_P	$\overline{CE}$ Precharge Time	35	–	40	–	50	–	ns	
t_{CEA}	$\overline{CE}$ Access Time	–	70	–	80	–	100	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	30	–	30	–	40	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	20	–	20	–	20	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	–	10	–	10	–	ns	9
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	–	0	–	0	–	ns	9
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{WP}	Write Pulse Width	25	–	25	–	30	–	ns	
t_{WCH}	Write Command Hold Time	40	–	40	–	50	–	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	25	–	25	–	30	–	ns	
t_{DSW}	Data Set-Up Time from R/W	20	–	20	–	25	–	ns	10
t_{DSC}	Data Set-Up Time from $\overline{CE}$	20	–	20	–	25	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	–	0	–	0	–	ns	10
t_{ASC}	Address Set-Up Time	0	–	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	15	–	20	–	25	–	ns	11
t_{FC}	Auto Refresh Cycle Time	115	–	130	–	160	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	35	–	40	–	50	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
t_{FRS}	$\overline{CE}$ Delay Time form $\overline{RFSH}$ (Self Refresh)	130	–	160	–	190	–	ns	12
t_{REF}	Refresh Period (2048 cycle, A0~A10)	–	32	–	32	–	32	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} and I_{DDF4} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up, before proper device operation is achieved.
6) AC measurements asuume t_T = 5ns.
7) Timing reference level

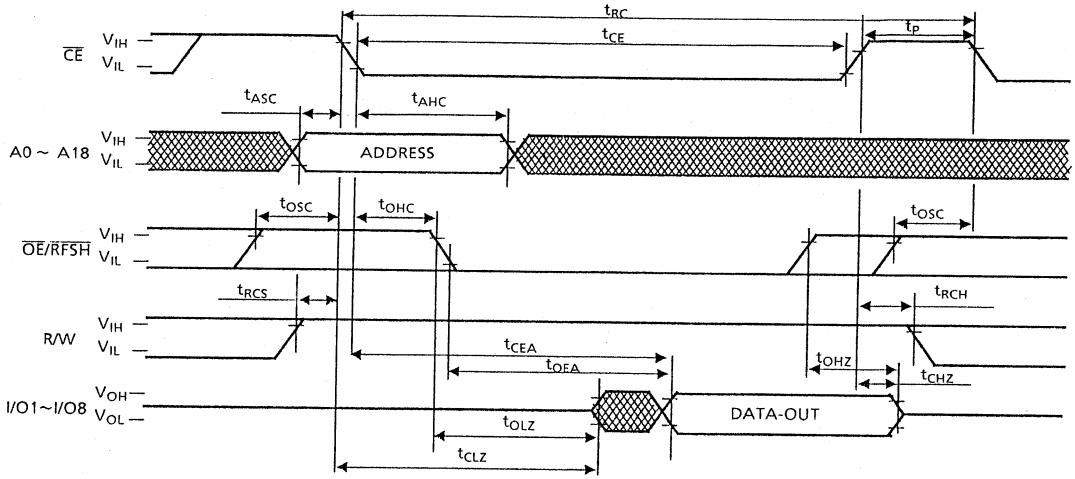
Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level	:	V_{OH} = 2.2V
		V_{OL} = 0.8V



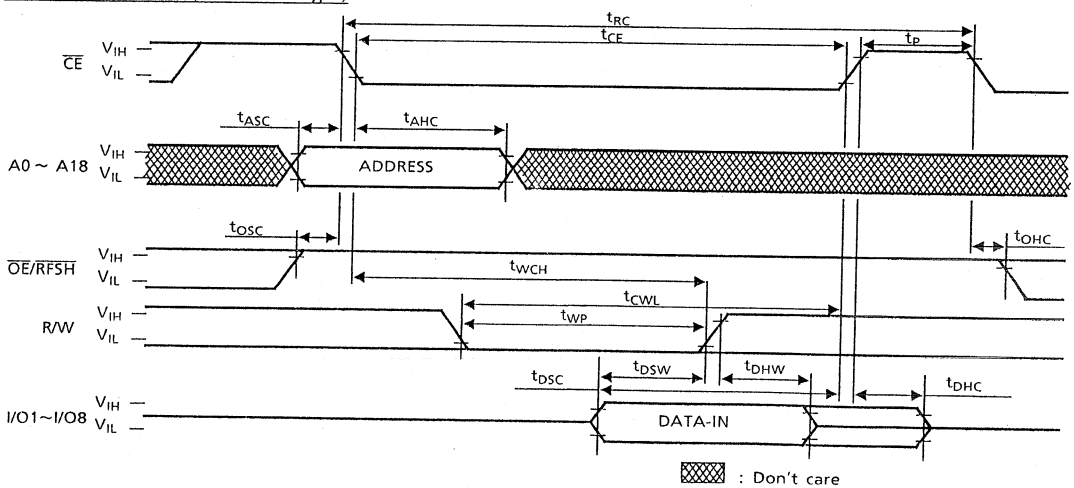
8) Measured with a load equivalent to 1 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore the all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE}$ = V_{IH}.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The timing parameter (t_{FRS}) must be kept for device proper operation in the following conditions.
    - after self refresh
    - in case of $\overline{OE}/\overline{RFSH}$ = "L" after power-up

TIMING WAVEFORMS

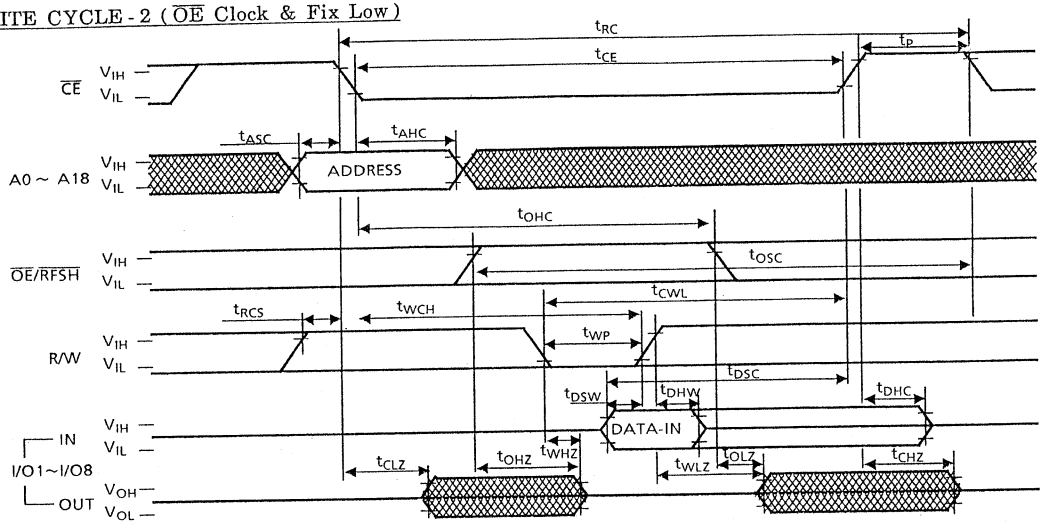
READ CYCLE



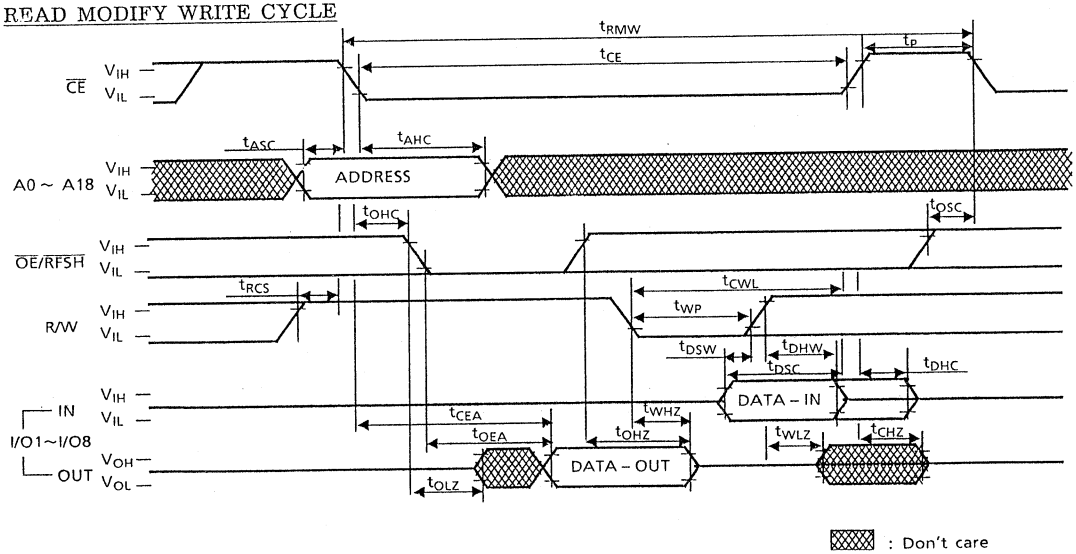
WRITE CYCLE-1 ($\overline{OE}$ Fix High)



WRITE CYCLE - 2 ($\overline{OE}$ Clock & Fix Low)

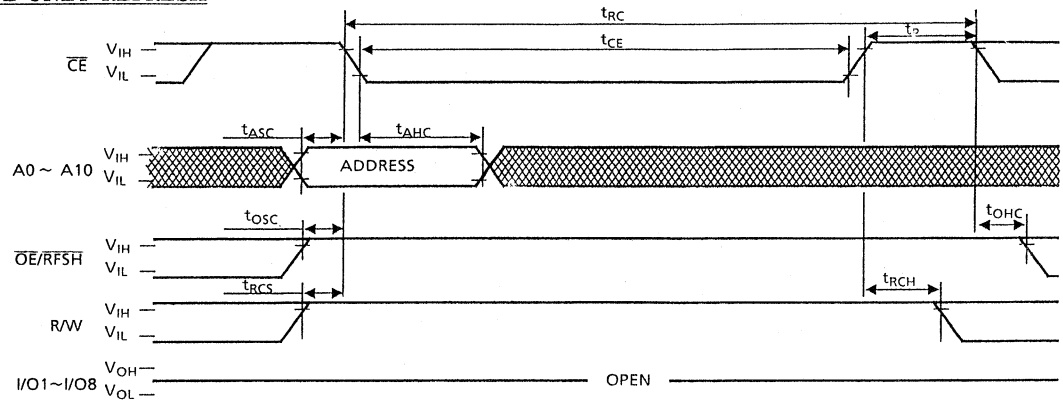


READ MODIFY WRITE CYCLE



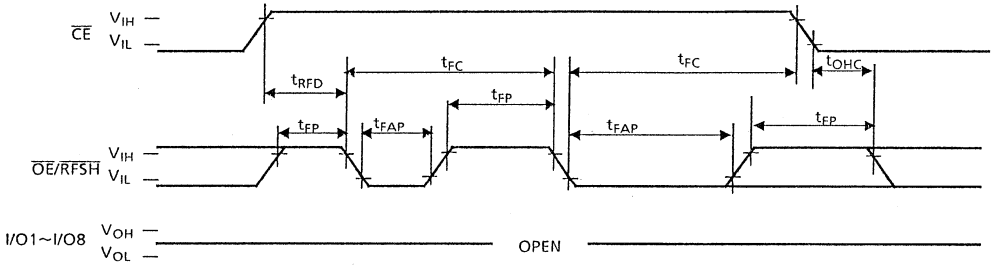
: Don't care

$\overline{CE}$ ONLY REFRESH



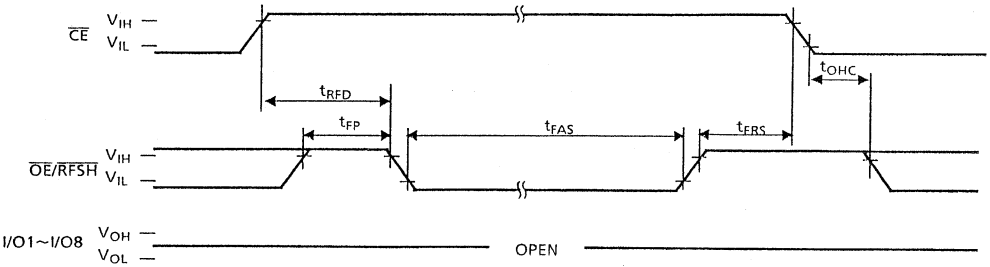
NOTE : A11 ~ A16 = Don't care, ▨ : Don't care

AUTO REFRESH



NOTE : R/W, A0 ~ A18 = Don't care

SELF REFRESH



NOTE : R/W, A0 ~ A18 = Don't care

TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

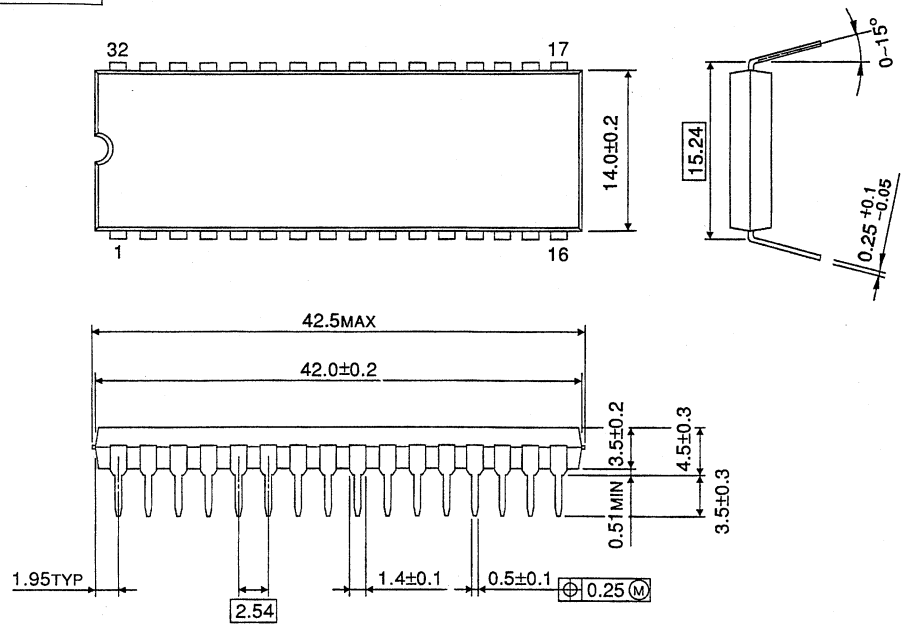
We hope this information will be very useful for you.

Nov. 1991

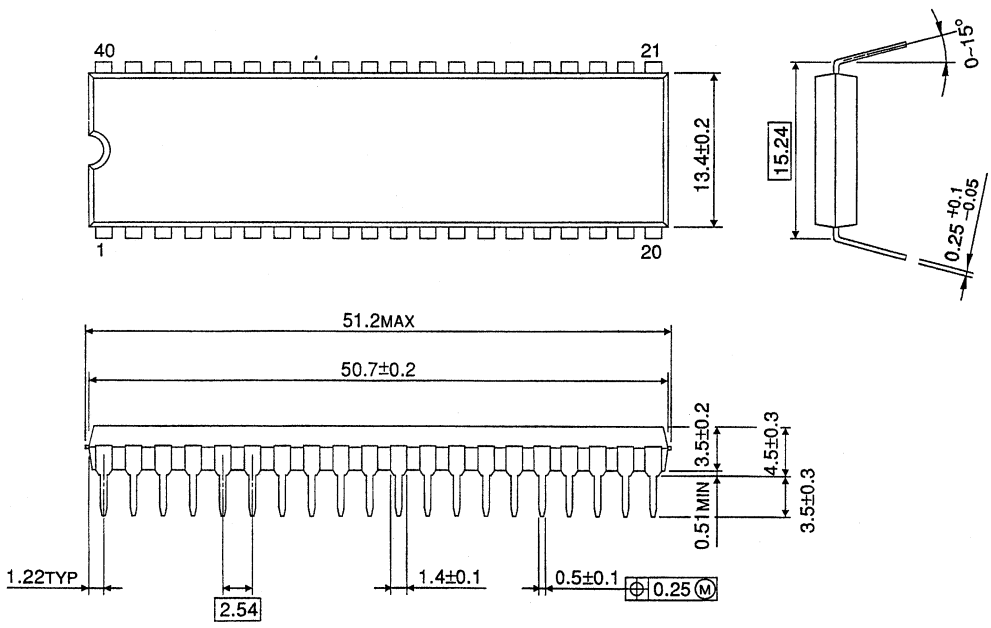
TOSHIBA CORPORATION
Semiconductor Group

Unit in mm

DIP32-P-600

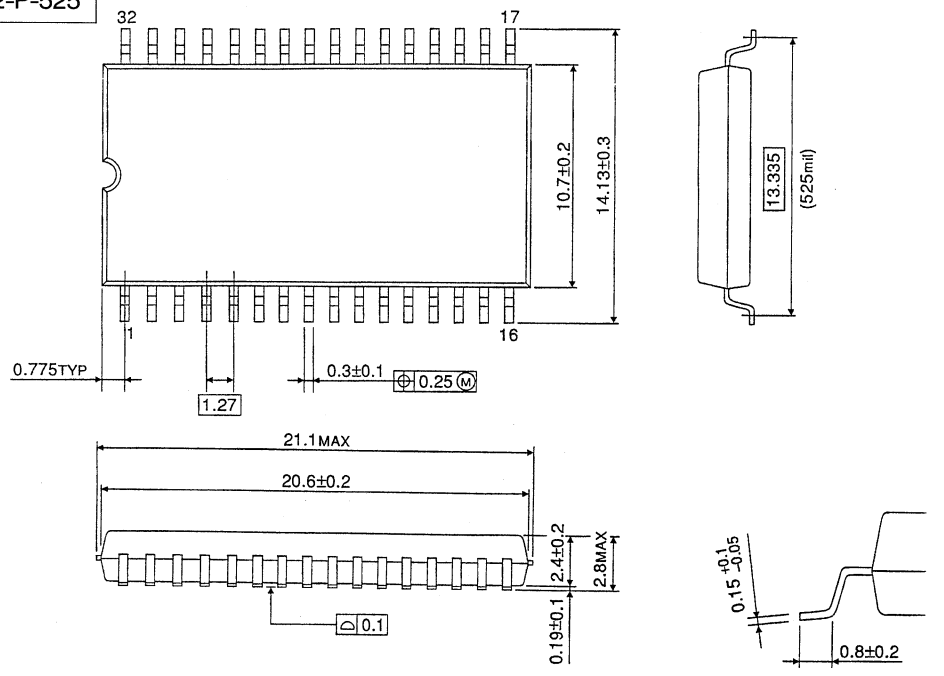


DIP40-P-600

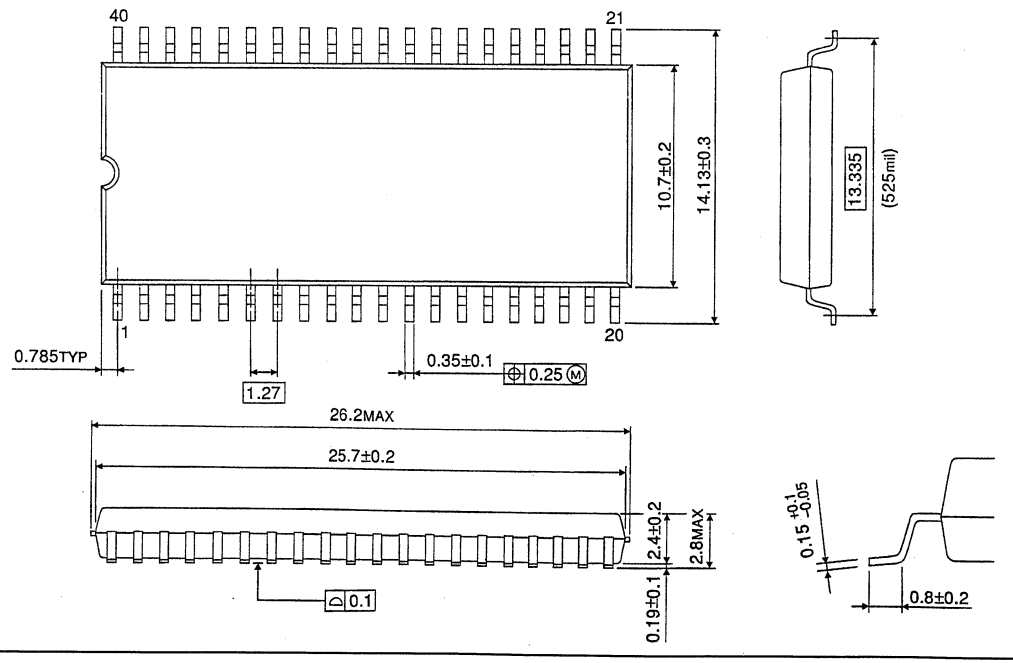


Unit in mm

SOP32-P-525



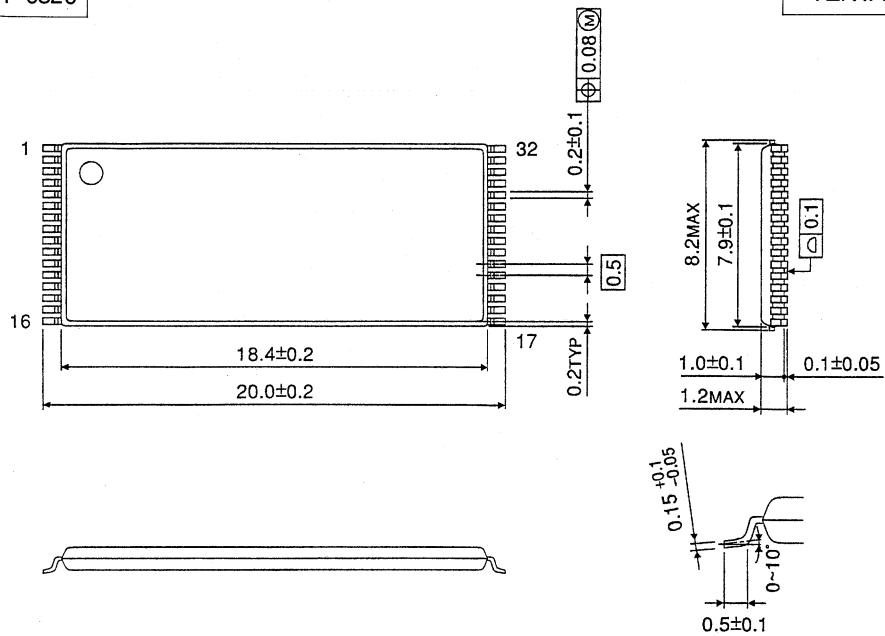
SOP40-P-525



Unit in mm

TSOP32-P-0820

TENTATIVE



TSOP32-P-0820A

TENTATIVE