TC528126BJ/BZ/BFT/BTR-80,-10

TENTATIVE DATA

131,072WORDS × 8BITS MULTIPORT DRAM

DESCRIPTION

The TC528126BJ / BZ / BFT / BTR is a CMOS multiport memory equipped with a 131,072-words by 8-bits dynamic random access memory (RAM) port and a 256-words by 8-bits static serial access memory (SAM) port. The TC528126BJ / BZ / BFT / BTR supports three types of operations; Random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. The TC528126BJ / BZ / BFT / BTR is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

ITEM		TC528126BJ / BZ / BFT / BTR -80	TC528126BJ / BZ / BFT / BTR -10
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	80ns	100ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	25ns	25ns
t_{AA}	Column Address Access Time (Max.)	45ns	50ns
t_{RC}	Cycle Time (Min.)	150ns	180ns
t_{PC}	Page Mode Cycle Time (Min.)	50ns	55ns
t_{SCA}	Serial Access Time (Max.)	25ns	25ns
t_{SCC}	Serial Cycle time (Min.)	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	90mA	75mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	50mA	50mA
I_{CC2}	Standby Current	10mA	10mA

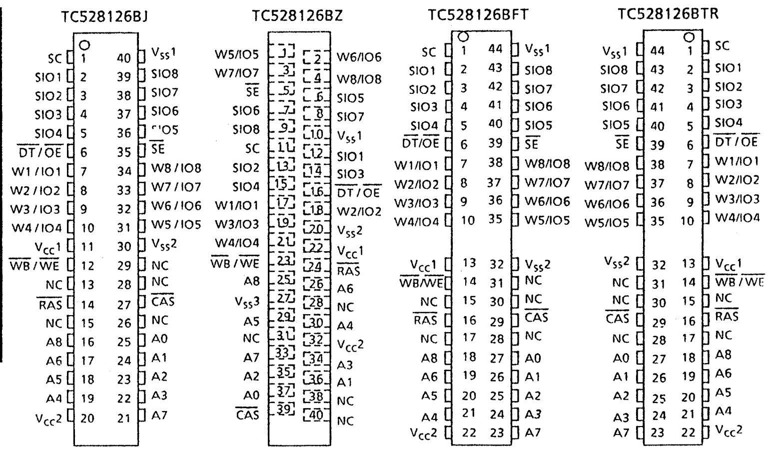
- Single power supply of 5V±10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible

- Organization
  - RAM Port : 131,072words × 8bits
  - SAM Port : 256words × 8bits
- RAM Port
  - Fast Page Mode, Read - Modify - Write
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh
  - $\overline{RAS}$ only Refresh, Write per Bit
  - 512 refresh cycles / 8ms
- SAM Port
  - High Speed Serial Read / Write Capability
  - 256 Tap Locations
  - Fully Static Register
- RAM - SAM Bidirectional Transfer
  - Read / Write / Pseudo Write Transfer
  - Real Time Read Transfer
- Package
  - TC528126BJ : SOJ40 - P - 400
  - TC528126BZ : ZIP40 - P - 475
  - TC528126BFT : TSOP44 - P - 400B
  - TC528126BTR : TSOP44 - P - 400C

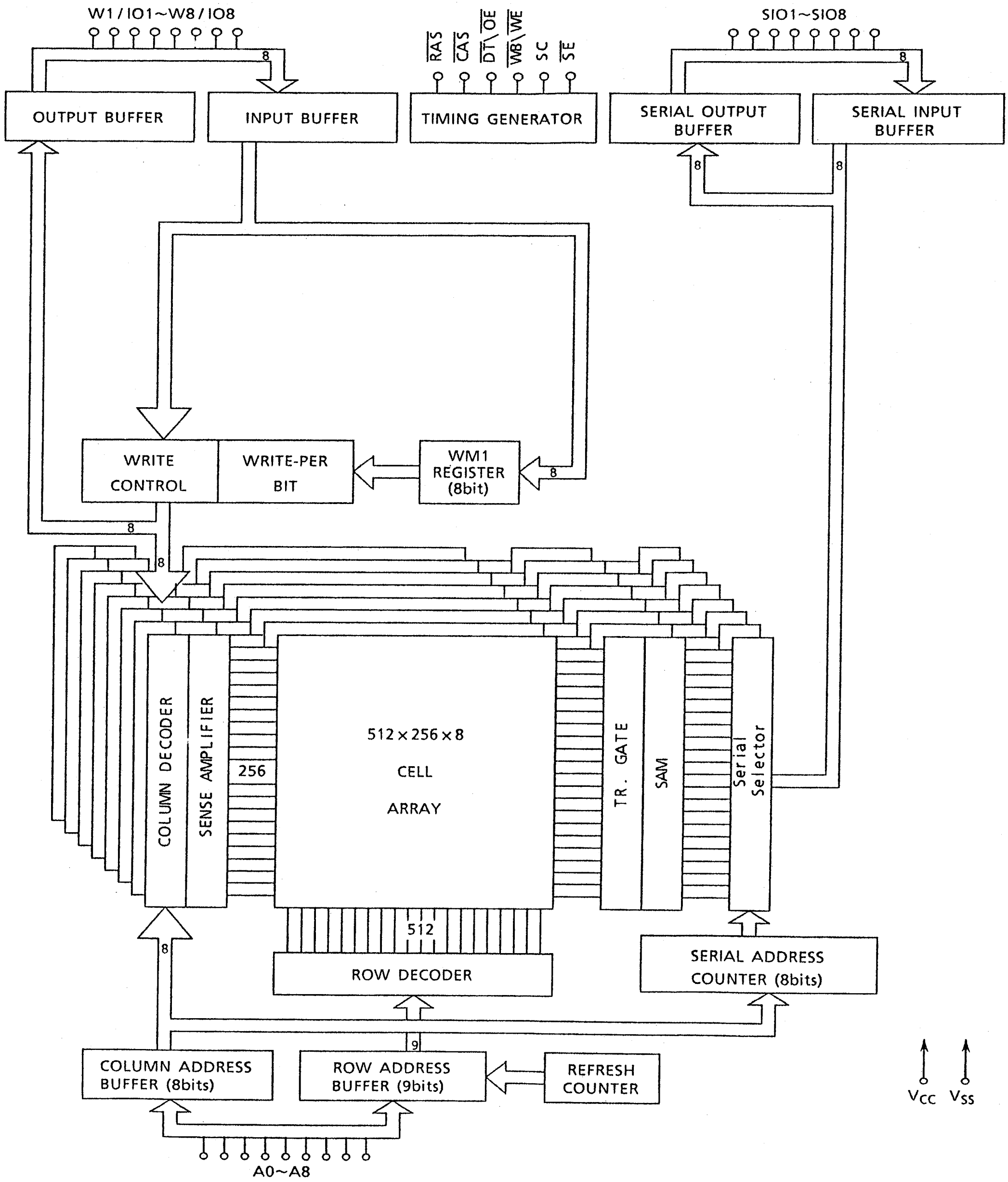
PIN NAME

A0~A8	Address inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}$ / $\overline{OE}$	Data Transfer / Output Enable
$\overline{WB}$ / $\overline{WE}$	Write per Bit / Write Enable
W1/IO1~W8/IO8	Write Mask / Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1~SIO8	Serial Input / Output
V_{CC} / V_{SS}	Power (5V) / Ground
N. C.	No Connection

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	– 1.0~7.0	V	1
V_{CC}	Power Supply Voltage	– 1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	– 55~150	°C	1
T_{SOLDER}	Soldering Temperature · Time	260·10	°C·sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	– 1.0	–	0.8	V	2

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	–	7	pF
C_{IO}	Input / Output Capacitance	–	9	

Note : This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	TC528126BJ/BZ/BFT/BTR-80		TC528126BJ/BZ/BFT/BTR-10		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.)	Standby	I_{CC1}	–	90	–	75	mA	3, 4
	Active	I_{CC1A}	–	130	–	115		3, 4
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS} = V_{IH}$)	Standby	I_{CC2}	–	10	–	10		
	Active	I_{CC2A}	–	50	–	50		3, 4
$\overline{RAS}$ ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$ $t_{RC} = t_{RC}$ min.)	Standby	I_{CC3}	–	90	–	75		3, 4
	Active	I_{CC3A}	–	130	–	115		3, 4
PAGE MODE CURRENT ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC}$ min.)	Standby	I_{CC4}	–	80	–	65		3, 4
	Active	I_{CC4A}	–	120	–	105		3, 4
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$ $t_{RC} = t_{RC}$ min.)	Standby	I_{CC5}	–	90	–	75		3, 4
	Active	I_{CC5A}	–	130	–	115		3, 4
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.)	Standby	I_{CC6}	–	110	–	95		3, 4
	Active	I_{CC6A}	–	150	–	135		3, 4

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V ≦ V_{IN} ≦ 6.5V, All other pins not under test = 0V	$I_{I(L)}$	– 10	10	μA	
OUTPUT LEAKAGE CURRENT 0V ≦ V_{OUT} ≦ 5.5V, Output Disable	$I_{O(L)}$	– 10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = – 2mA	V_{OH}	2.4	–	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2mA	V_{OL}	–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes : 5, 6, 7)

SYMBOL	PARAMETER	TC528126BJ / BZ / BFT / BTR-80		TC528126BJ / BZ / BFT / BTR-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150		180			
t_{RMW}	Read - Modify - Write Cycle Time	195		235			
t_{PC}	Fast Page Mode Cycle Time	50		55			
t_{PRMW}	Fast Page Mode Read - Modify - Write Cycle Time	90		100			
t_{RAC}	Access Time from $\overline{RAS}$		80		100		8,14
t_{AA}	Access Time from Column Address		45		50		8,14
t_{CAC}	Access Time from $\overline{CAS}$		25		25		8,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		8,15
t_{OFF}	Output Buffer Turn - Off Delay	0	20	0	20		10
t_T	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	60		70			
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10000	100	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	80	100000	100	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	25		25			
t_{CSH}	$\overline{CAS}$ Hold Time	80		100		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10000	25	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	55	20	75		14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	50		14
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45		50			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set - Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set - Up Time	0		0			
t_{CAH}	Column Address Hold Time	15		15			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55		70			
t_{RCS}	Read Command Set - Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			11
t_{WCH}	Write Command Hold Time	15		15			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55		70			
t_{WP}	Write Command Pulse Width	15		15			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25			

SYMBOL	PARAMETER	TC528126BJ / BZ / BFT / BTR-80		TC528126BJ / BZ / BFT / BTR-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DS}	Data Set-Up Time	0		0		ns	12
t_{DH}	Data Hold Time	15		15			12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55		70			
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100		130			13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65		80			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		55			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		20		25		8
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	10	0	20		10
t_{OED}	$\overline{OE}$ to Data Delay Time	10		20			
t_{OEH}	$\overline{OE}$ Command Hold Time	10		20			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	15		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	15		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10000	15	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	65	10000	80	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	30		30			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	25		25			

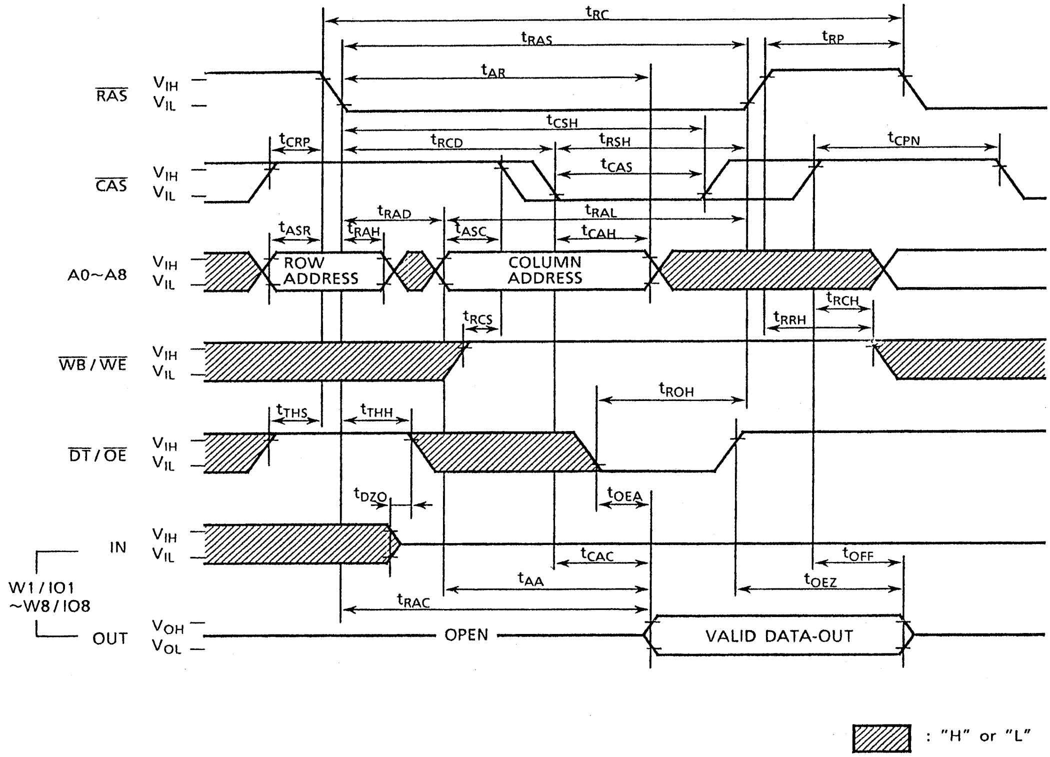
SYMBOL	PARAMETER	TC528126BJ / BZ / BFT / BTR-80		TC528126BJ / BZ / BFT / BTR-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60		70			
t_{TP}	$\overline{DT}$ Precharge Time	20		30			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	80		100			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	45		50			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	25		25			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		50			
t_{SDZ}	Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	50		10
t_{SCC}	SC Cycle Time	30		30			
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	10		10			
t_{SCA}	Access Time from SC		25		25		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	15		15			
t_{SEA}	Access Time from $\overline{SE}$		25		25		9
t_{SE}	$\overline{SE}$ Pulse Width	25		25			
t_{SEP}	$\overline{SE}$ Precharge Time	25		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0	20	0	20		10
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	15		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	15		15			

NOTES :

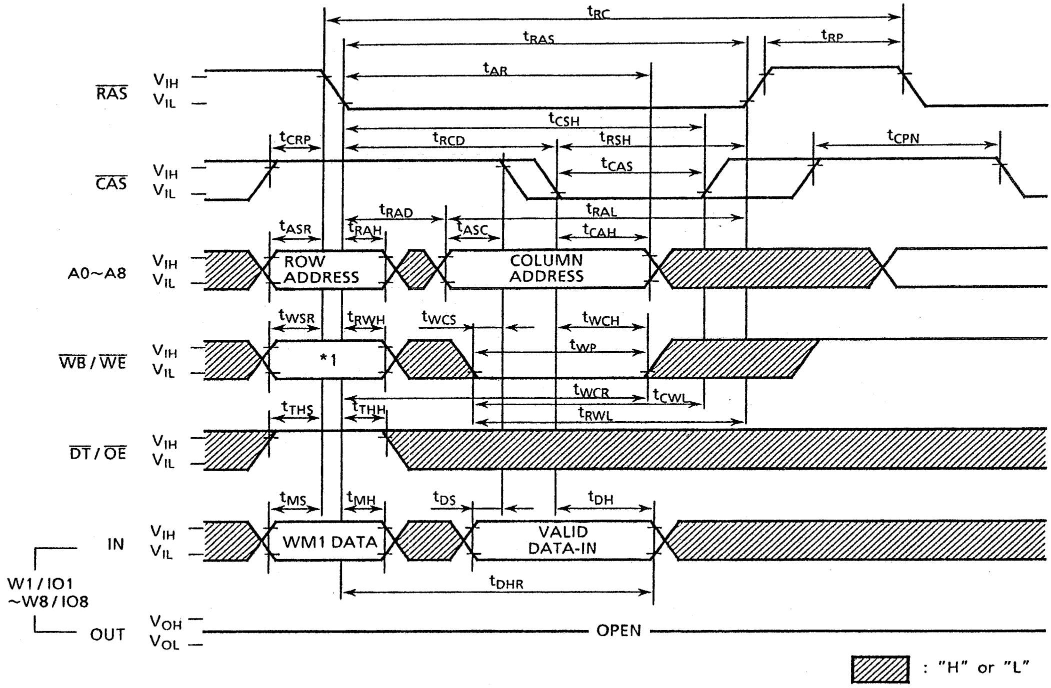
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. These parameters depend on cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5$ns.
7. $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. RAM port outputs are measured with a load equivalent to 1 TTL load and 100pF. D_{OUT} reference levels : $V_{OH}/V_{OL} = 2.0V/0.8V$.
9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF. D_{OUT} reference levels : $V_{OH}/V_{OL} = 2.0V/0.8V$.
10. $t_{OFF\,(max.)}$, $t_{OEZ\,(max.)}$, $t_{SDZ\,(max.)}$ and $t_{SEZ\,(max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycle and read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS\,(min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; If $t_{RWD} \geqq t_{RWD\,(min.)}$, $t_{CWD} \geqq t_{CWD\,(min.)}$ and $t_{AWD} \geqq t_{AWD\,(min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RCD\,(max.)}$ is specified as a reference point only : If t_{RCD} is greater than the specified $t_{RCD\,(max.)}$ limit, then access time is controlled by t_{CAC}.
15. Operation within the $t_{RAD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only : If t_{RAD} is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by t_{AA}.

TIMING WAVEFORM

READ CYCLE



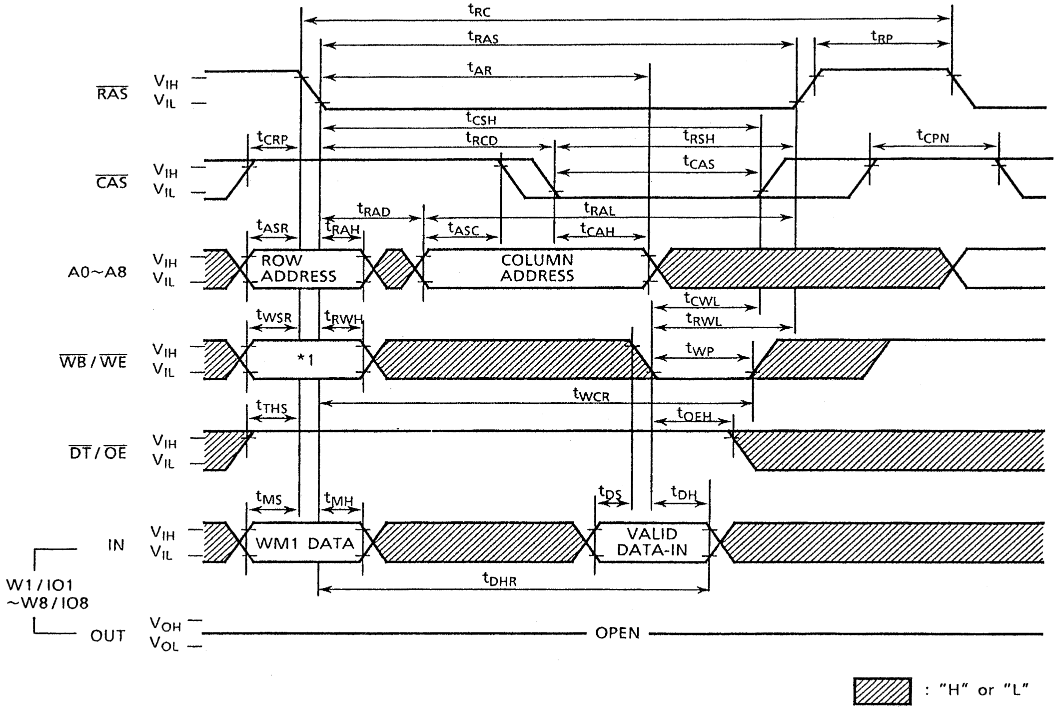
WRITE CYCLE (EARLY WRITE)



*1 WB / WE	W1 / IO1~W8 / IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

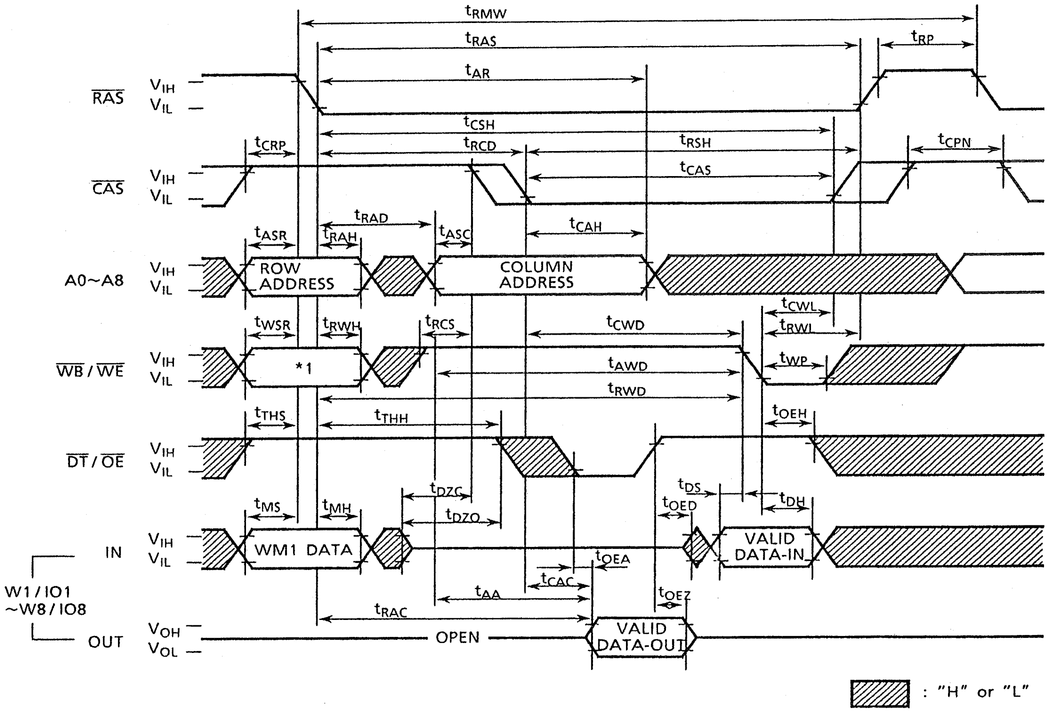
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



*1 $\overline{WB}$ / $\overline{WE}$	W1 / IO1~W8 / IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

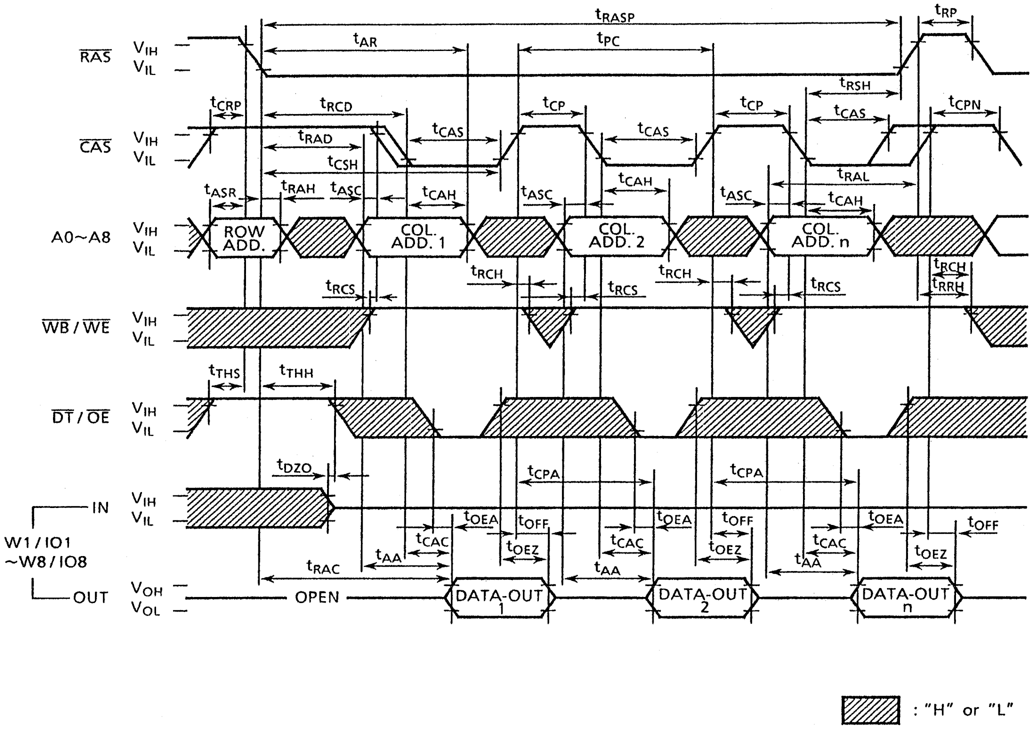
READ - MODIFY - WRITE CYCLE



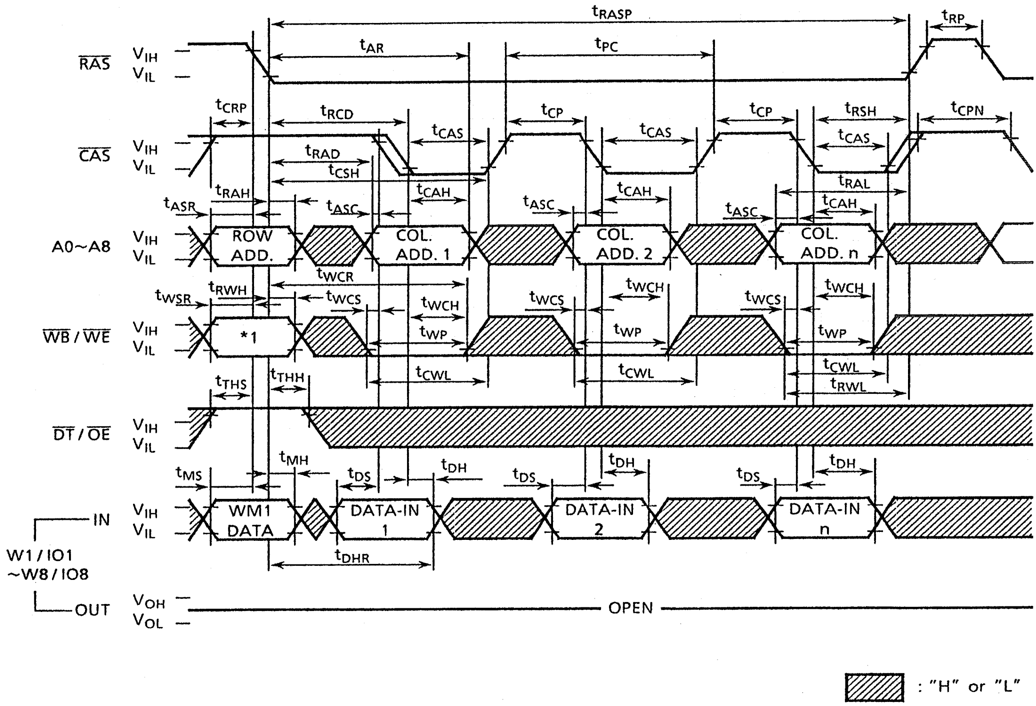
*1 $\overline{WB}$ / $\overline{WE}$	W1 / IO1~W8 / IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

FAST PAGE MODE READ CYCLE



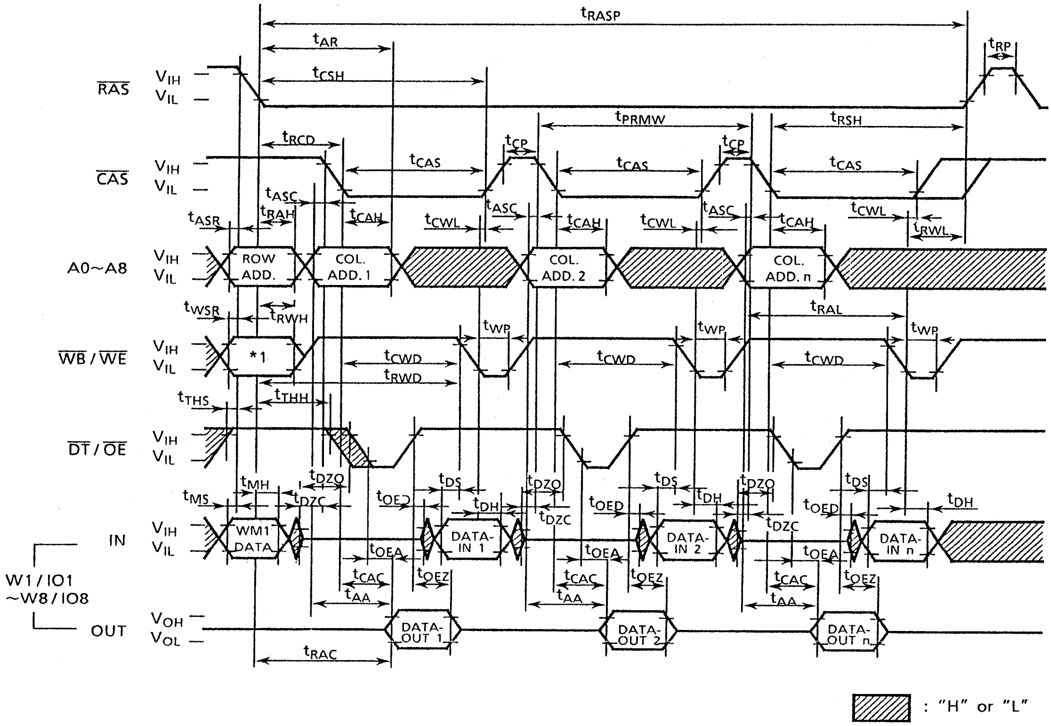
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



*1 $\overline{\text{WB}}$ / $\overline{\text{WE}}$	W1 / IO1~W8 / IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

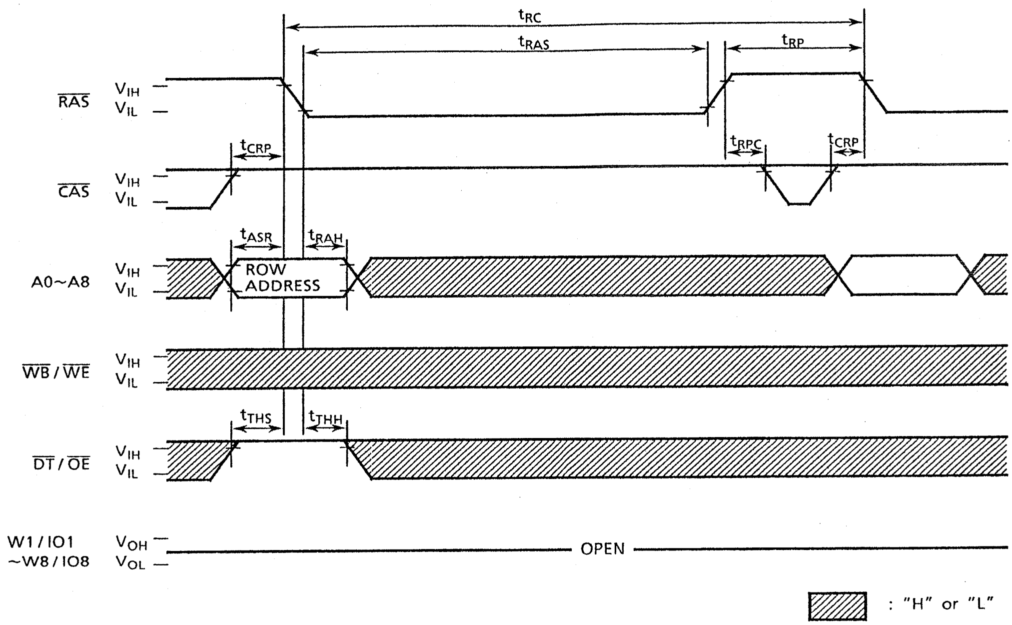
FAST PAGE MODE READ - MODIFY - WRITE CYCLE



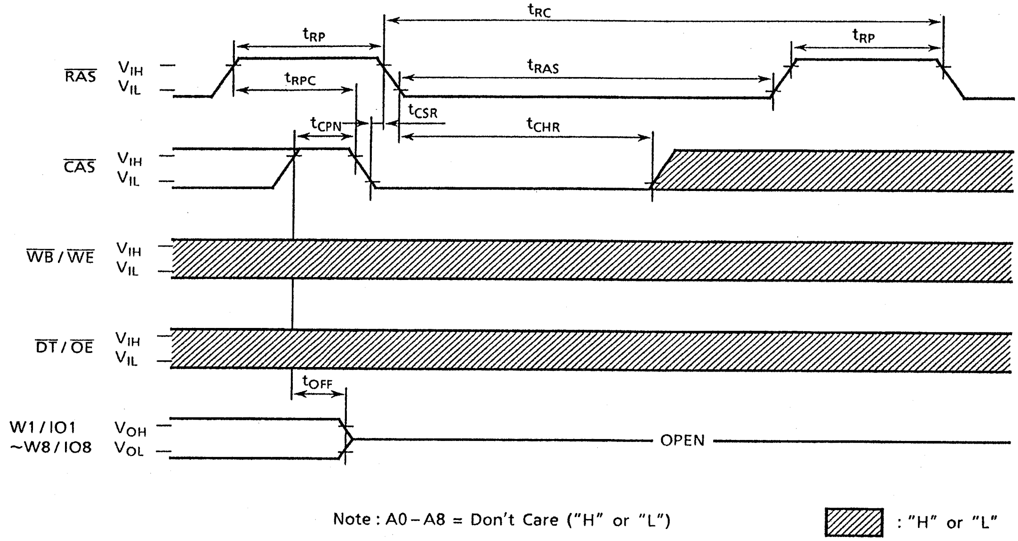
*1 $\overline{WB}$ / $\overline{WE}$	W1 / IO1~W8 / IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

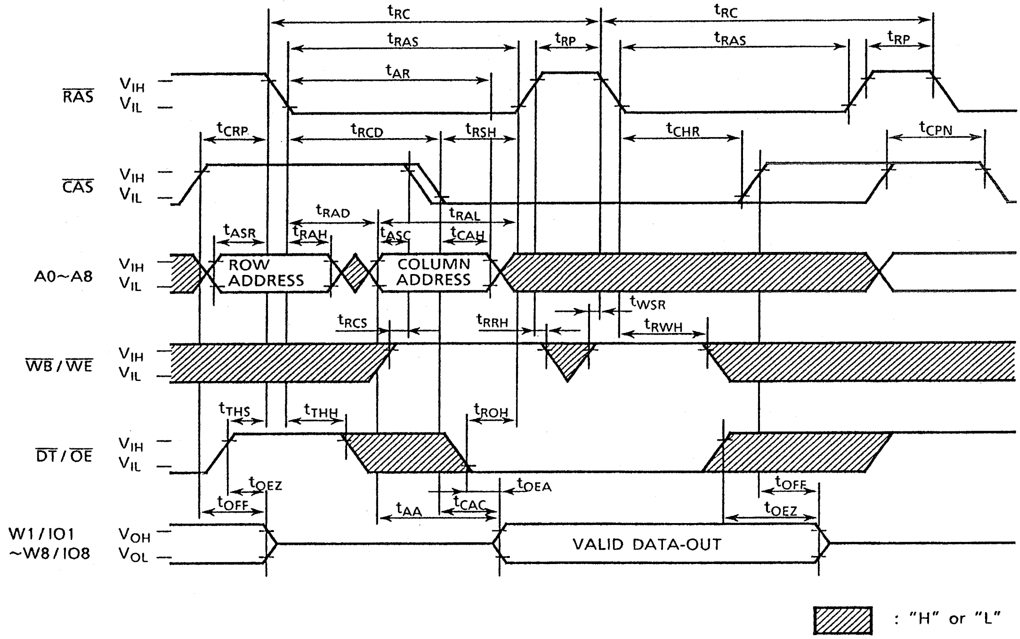
RAS ONLY REFRESH CYCLE



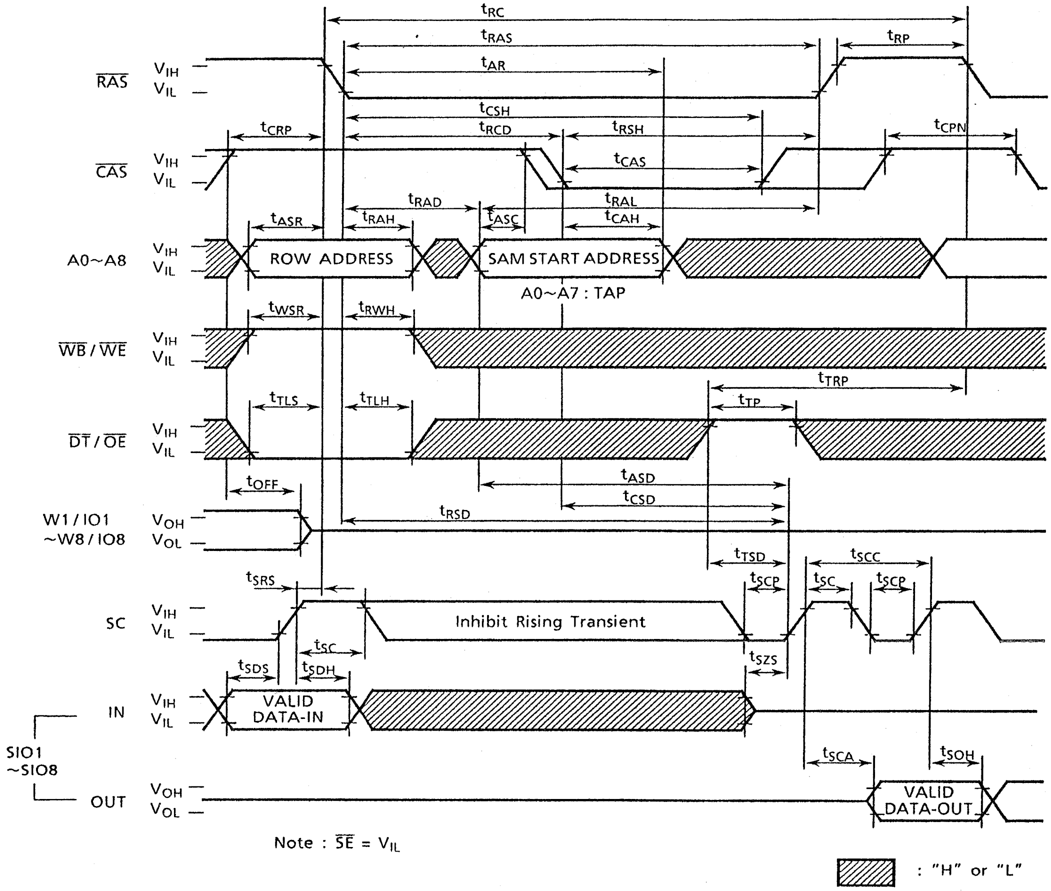
CAS BEFORE RAS REFRESH CYCLE



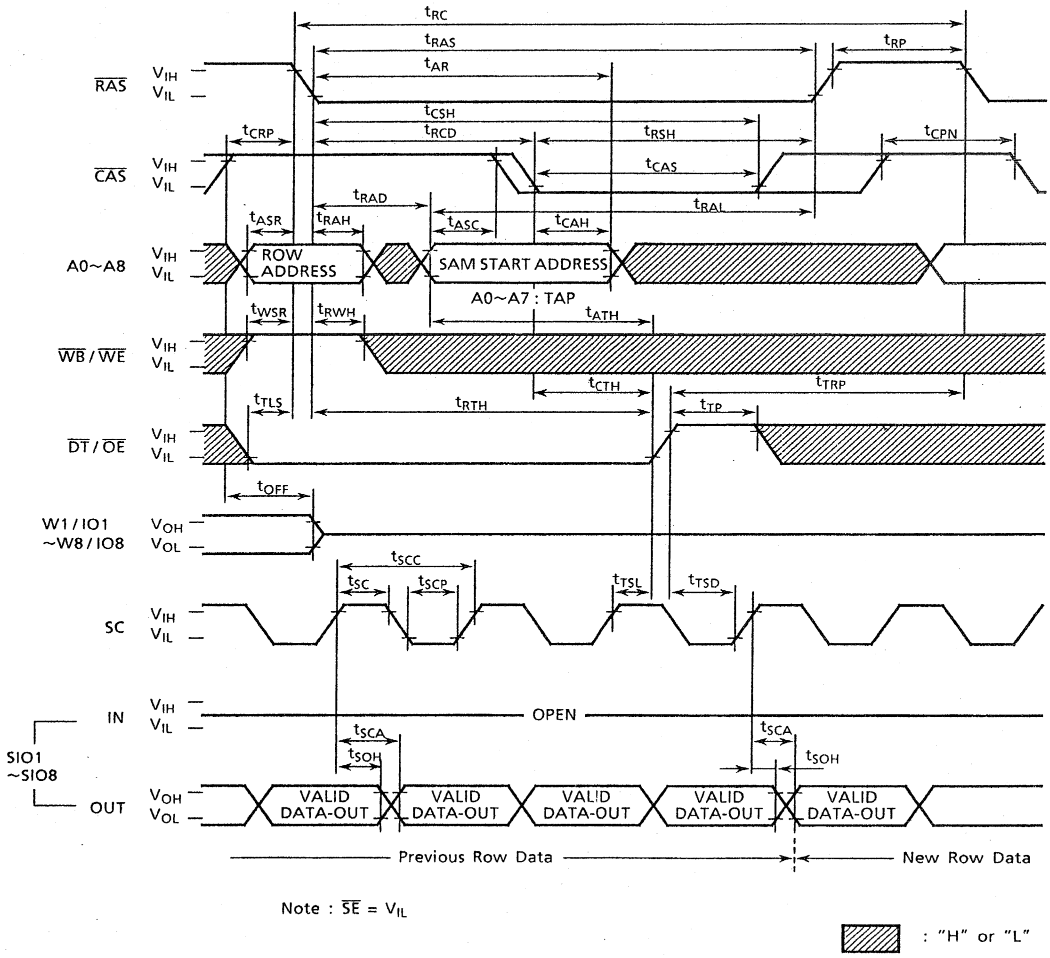
HIDDEN REFRESH CYCLE



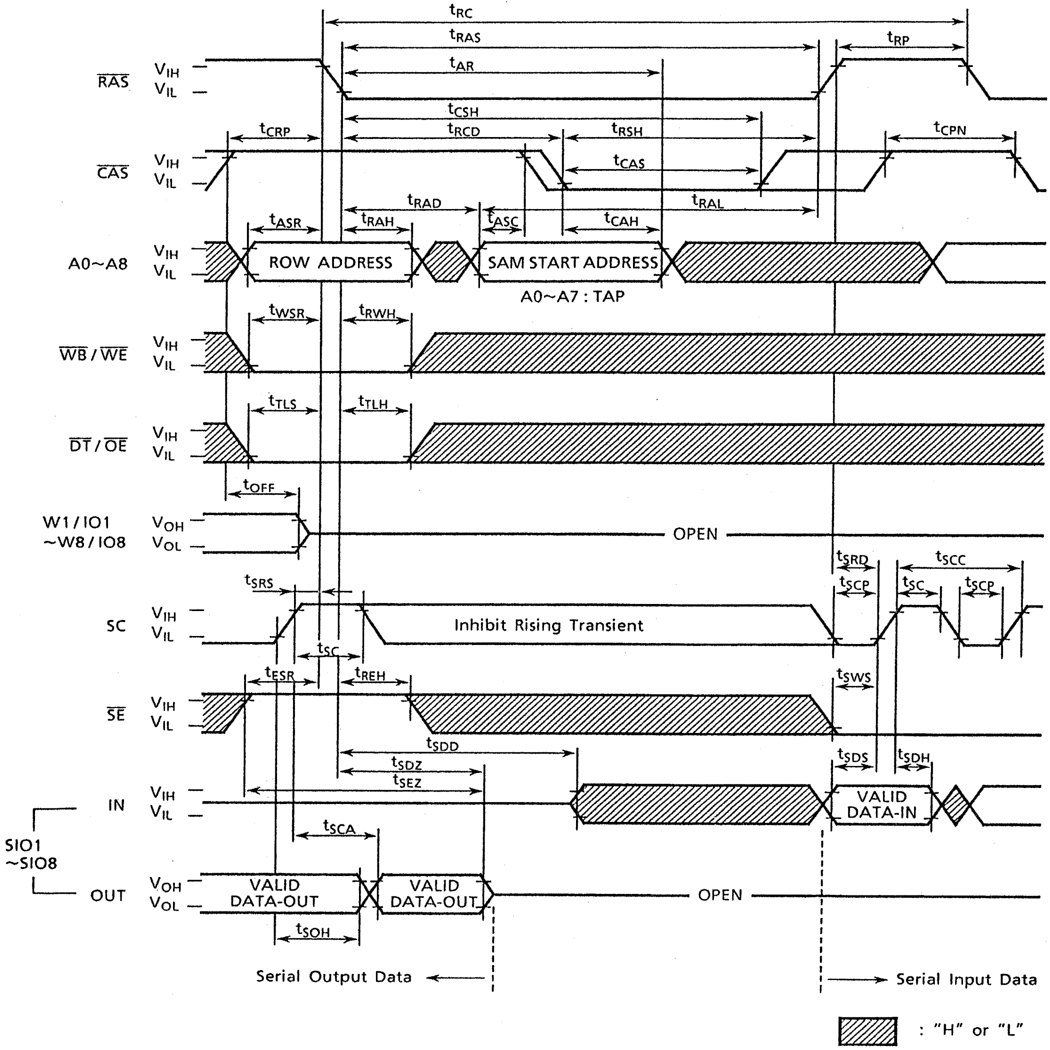
READ TRANSFER CYCLE (Previous Transfer is WRITE TRANSFER CYCLE)



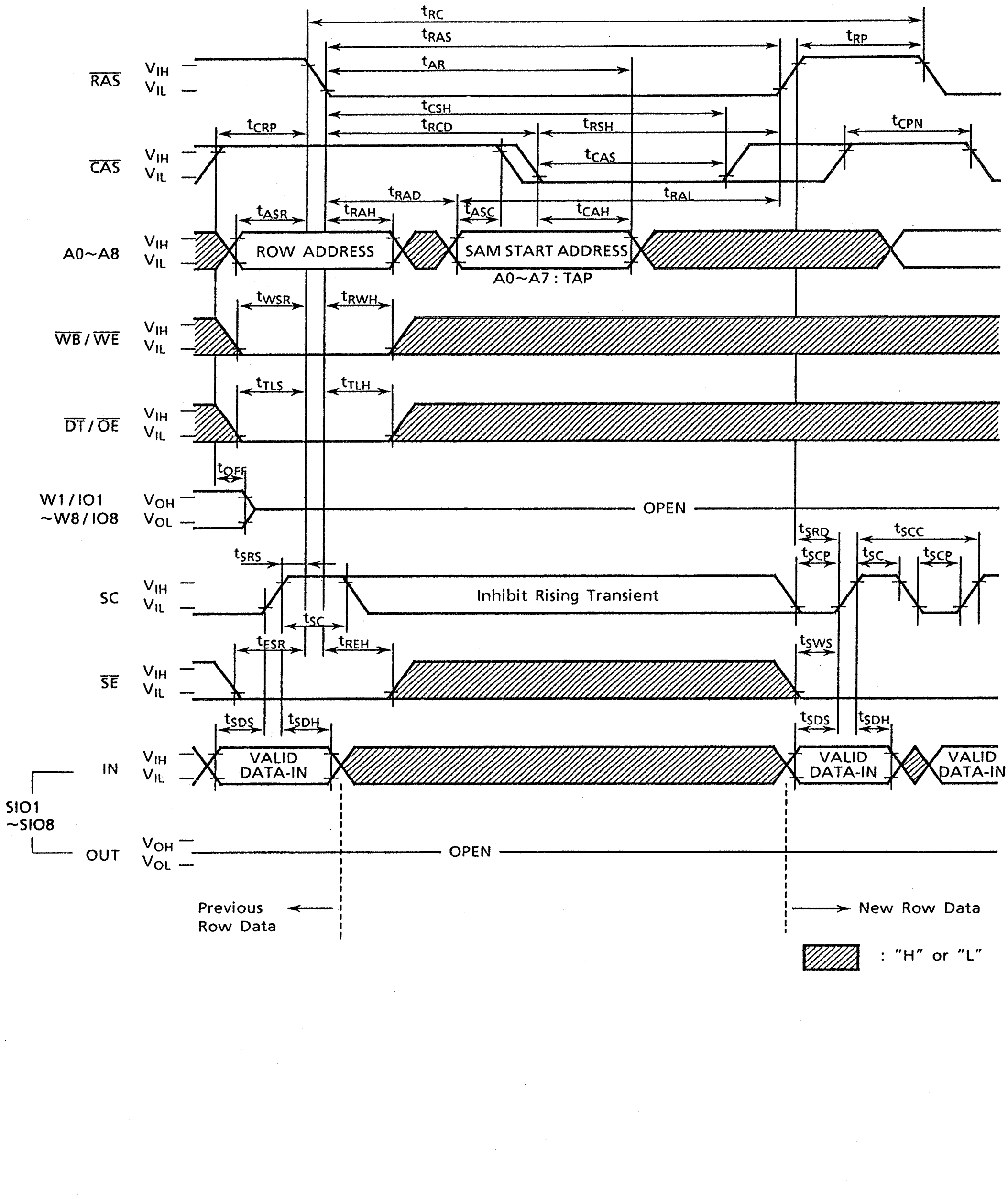
REAL TIME READ TRANSFER CYCLE



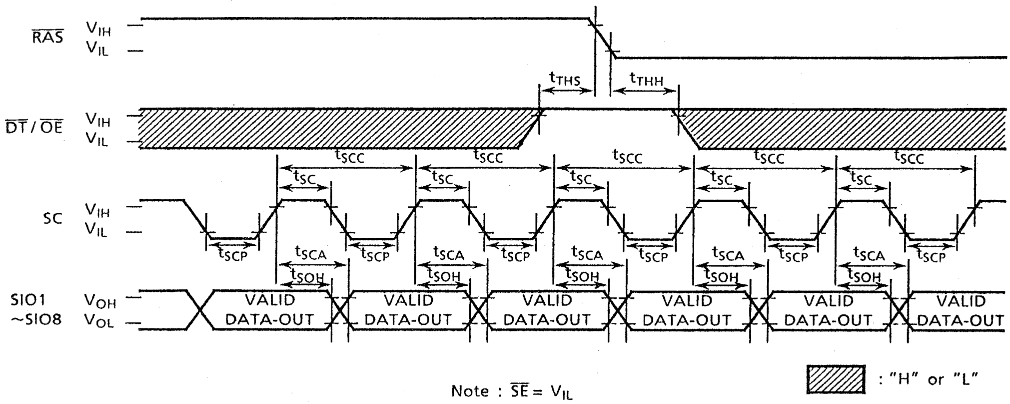
PSEUDO WRITE TRANSFER CYCLE



WRITE TRANSFER CYCLE



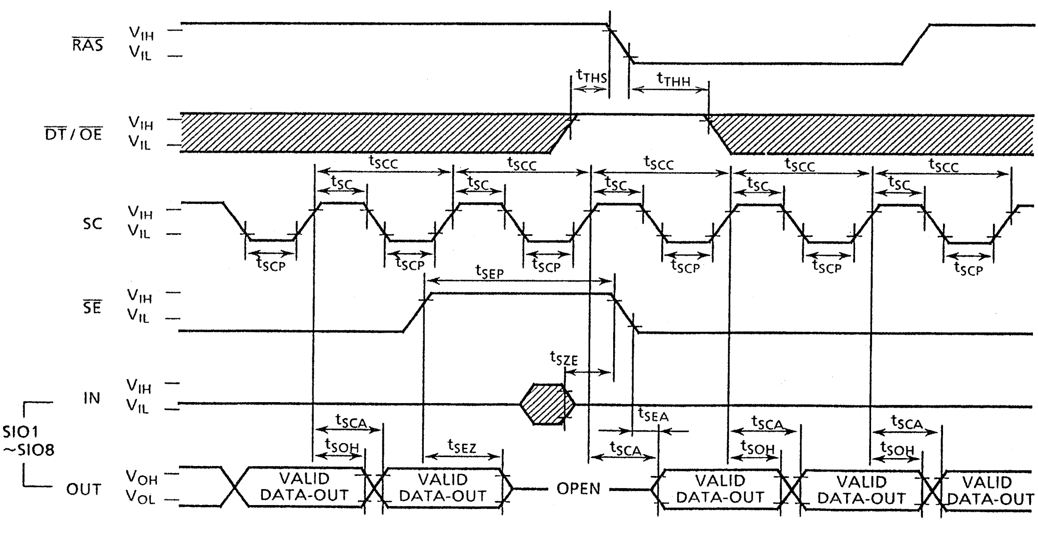
SERIAL READ CYCLE ($\overline{SE}=V_{IL}$)



Note : $\overline{SE}=V_{IL}$

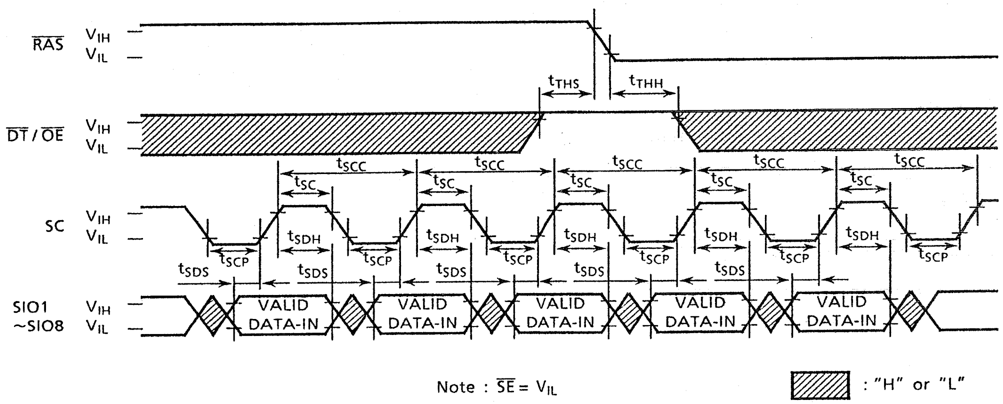
: "H" or "L"

SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)

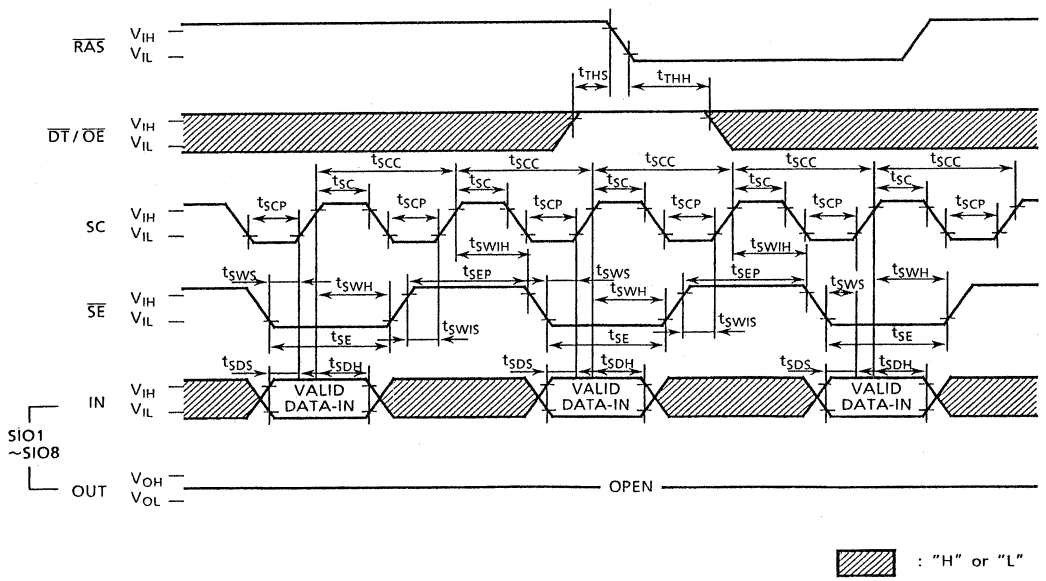


: "H" or "L"

SERIAL WRITE CYCLE ($\overline{SE}$ = V_{IL})



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

ADDRESS INPUTS : $A_0 \sim A_8$

The 17 address bits required to decode 8 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the TC528126BJ / BZ / BFT / BTR are multiplexed onto 9 address input pins ($A_0 \sim A_8$).
Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following eight column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ to invoke the various random access and data transfer operating modes shown in Table 2.
$\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

DATA TRANSFER / OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. When the $\overline{DT}/\overline{OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE PER BIT / WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).
When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write transfer).

WRITE MASK DATA / DATA INPUT AND OUTPUT : W_1/IO_1~W_8/IO_8

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$, whichever occurs first.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 8-bits serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 255), the next SC clock will place it at the least significant address location (decimal 0).
The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read transfer / pseudo write transfer / write transfer operations and should not be clocked while the SAM port is in the standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

SERIAL INPUT / OUTPUT : SIO1~SIO8

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During subsequent write transfer cycle, the SAM remains in the input mode.

OPERATION MODE

The RAM port and data transfer operating of the TC528126BJ / BZ / BFT / BTR are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ at the falling edge of $\overline{RAS}$. The Table 1 and the Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operation, respectively.

Table 1. Operation Truth Table

$\overline{RAS}$ falling edge ↓				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	
0	*	*	*	$\overline{CAS}$ before $\overline{RAS}$ Refresh
1	0	0	0	Write Transfer
1	0	0	1	Pseudo Write Transfer
1	0	1	*	Read Transfer
1	1	0	*	Read / Write per Bit
1	1	1	*	Read / Write

Table 2. Functional Truth Table

Function	$\overline{RAS}$ ↓				Address		W / IO		Write Mask
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓ $\overline{WE}$ ↓	WM1
$\overline{CAS}$ before $\overline{RAS}$ Refresh	0	*	*	*	*	–	*	–	–
Write Transfer	1	0	0	0	Row	TAP	*	*	–
Pseudo Write Transfer	1	0	0	1	Row	TAP	*	*	–
Read Transfer	1	0	1	*	Row	TAP	*	*	–
Write per Bit	1	1	0	*	Row	Column	WM1	DIN	Load use
Read / Write	1	1	1	*	Row	Column	*	DIN	–

* : "0" or "1" , TAP : SAM start address , – : not used

RAM PORT OPERATION

FAST PAGE MODE CYCLE

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{\text{CAS}}$ cycle during a single active $\overline{\text{RAS}}$ cycle. During a fast page cycle, the $\overline{\text{RAS}}$ signal may be maintained active for a period up to 100 μseconds. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, column address and $\overline{\text{DT}}/\overline{\text{OE}}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{\text{CAS}}$, column address and $\overline{\text{DT}}/\overline{\text{OE}}$. When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{\text{RAS}}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{\text{RAS}}$-ONLY REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{\text{RAS}}$-Only" cycle.

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH

The TC528126BJ / BZ / BFT / BTR also offers an internal-refresh function. When $\overline{\text{CAS}}$ is held "low" for a specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle. For successive $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle, $\overline{\text{CAS}}$ can remain "low" while cycling $\overline{\text{RAS}}$.

HIDDEN REFRESH

A hidden refresh is a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh performed by holding $\overline{\text{CAS}}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{\text{RAS}}$ after the specified $\overline{\text{RAS}}$-precharge period (Refer to Figure 1).

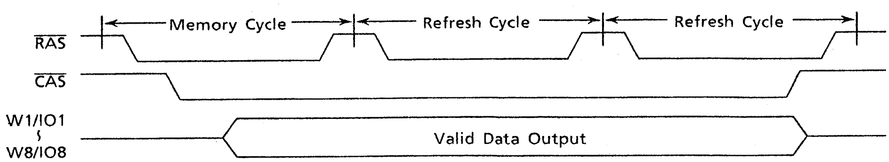


Figure 1. Hidden Refresh Cycle

WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the W_i/IO_i pins is latched onto the write-mask register (WM1). When a "0" is sensed on any of the W_i/IO_i pins, their corresponding write circuits are disabled and new data will not be written. When a "1" is sensed on any of the W_i/IO_i pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

Table 3. Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	W_i/IO_i (i = 1~8)	
H	H	H	*	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

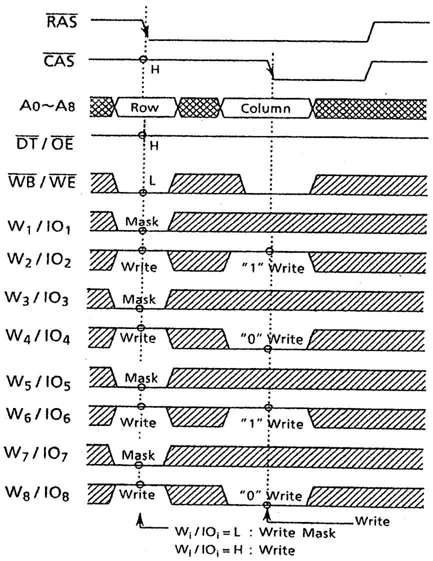


Figure 2. Write-per-bit timing cycle

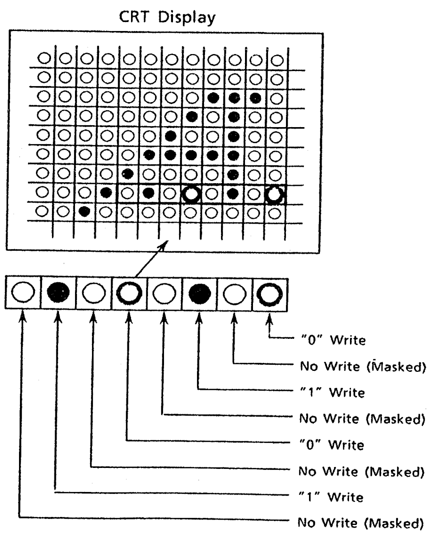
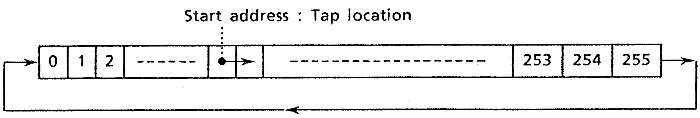


Figure 3. Corresponding bit-map

SAM PORT OPERATION

The TC528126BJ / BZ / BFT / BTR is provided with a 256 words by 8 bits serial access memory (SAM).
High speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read transfer / write transfer / pseudo-write transfer cycles.
The preceding transfer operation determines the direction of data flow through the SAM port.
If the preceding transfer operation is a read transfer, the SAM port is in the output mode.
If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; Data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM→SAM) has been performed. The data is shifted out of the SAM port starting at any of the 256 bits locations.
The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below.



Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

Table 4. Truth Table for SAM Port Operation

SAM PORT OPERATION	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	FUNCTION	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
Serial Output Mode	H	⎍	H	Disable Serial Read	Read Transfer
Serial Input Mode	H	⎍	L	Enable Serial Write	Write Transfer
Serial Input Mode	H	⎍	H	Disable Serial Write	Write Transfer
Serial Input Mode	H	⎍	L	Enable Serial Write	Pseudo Write Transfer
Serial Input Mode	H	⎍	H	Disable Serial Write	Pseudo Write Transfer

REFRESH

The SAM data registers are static flip-flop, therefore a refresh is not required.

DATA TRANSFER OPERATION

The TC528126BJ / BZ / BFT / BTR features internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 4. During a transfer, 256 words by 8 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer).

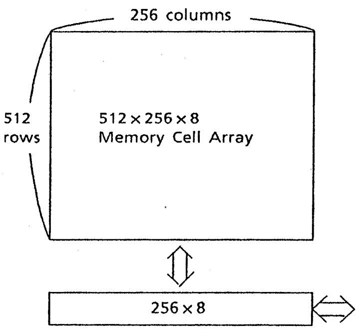


Figure 4. Data Transfer

As shown in Table 5, the TC528126BJ / BZ / BFT / BTR supports three types of transfer operations: Read transfer, Write transfer and Pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ latched at the falling edge of $\overline{RAS}$. During data transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer / Pseudo write transfer). During a data transfer cycle, the row address $A_0 \sim A_8$ select one of the 512 rows of the memory array to or from which data will be transferred and the column address $A_0 \sim A_7$ select one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle.

Table 5. Transfer Modes

at the falling edge of $\overline{RAS}$				Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$				
H	L	H	*	Read Transfer	RAM → SAM	256×8	Input → Output
H	L	L	L	Write Transfer	SAM → RAM	256×8	Output → Input
H	L	L	H	Pseudo Write Transfer	–	–	Output → Input

* : "H" or "L"

READ TRANSFER CYCLE

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" and $\overline{WB}/\overline{WE}$ "high" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read / real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 5 shows the operation block diagram for read transfer operation.

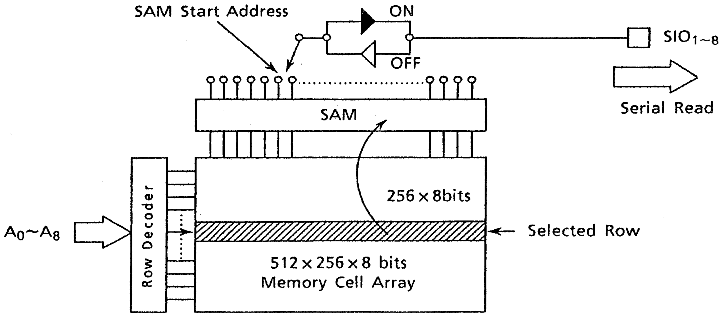


Figure 5. Block Diagram for Read Transfer Operation

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$, as shown in Figure 6.

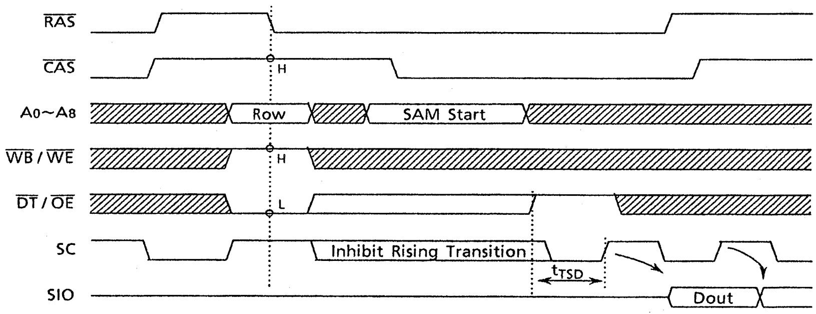


Figure 6. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time t_{SCA} for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 7.
The timing restriction t_{TSL}/t_{TSD} are 5ns min / 15ns min.

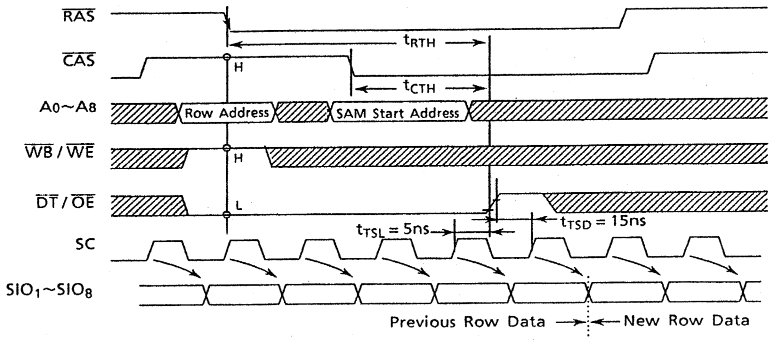


Figure 7. Real Time Read Transfer

WRITE TRANSFER CYCLE

A write transfer cycle consist of loading the content of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low" and $\overline{SE}$ "low" at the falling edge of $\overline{RAS}$.

Figure 8 and 9 show the timing diagram and block diagram for write transfer operations, respectively.

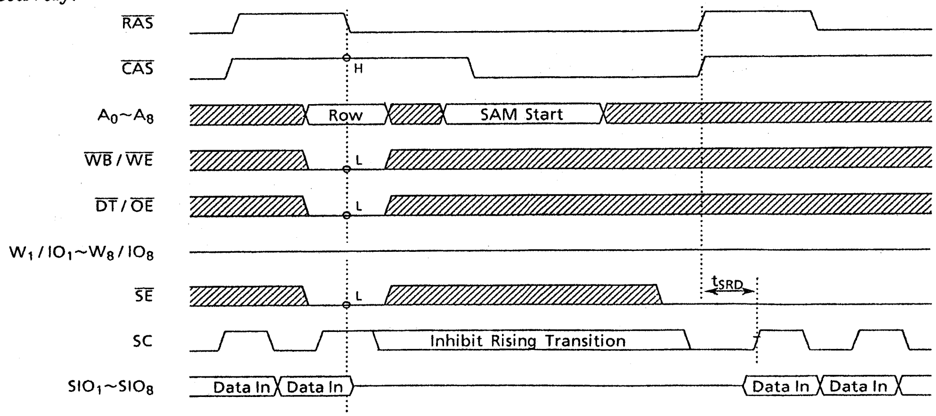


Figure 8. Write Transfer Timing

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

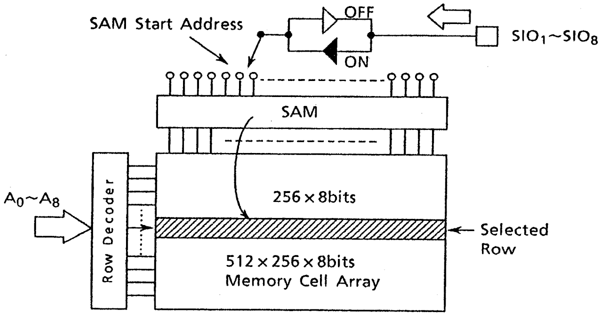


Figure 9. Block Diagram for Write Transfer Operation

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

PSEUDO WRITE TRANSFER CYCLE

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low" and $\overline{SE}$ "high" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

REGISTER OPERATION SEQUENCE (EXAMPLE)

Figure 10 illustrates an example of register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 255) and wraps around to the least significant address location. The SAM address is incremented as long as SC is clocked.

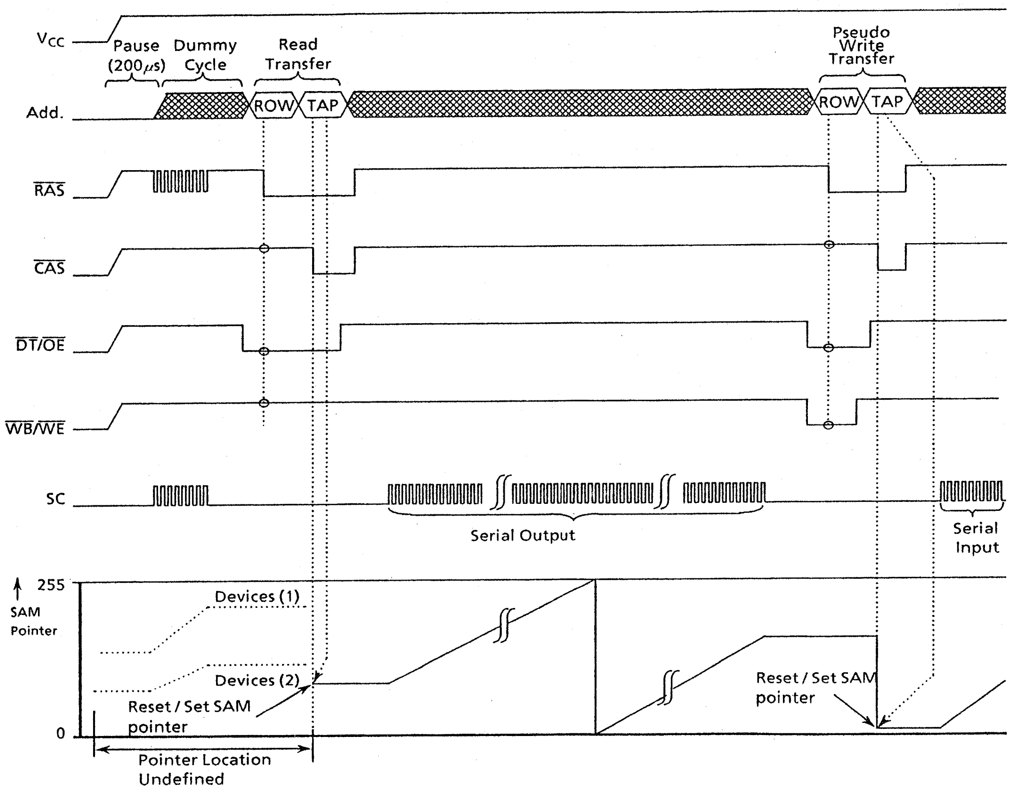
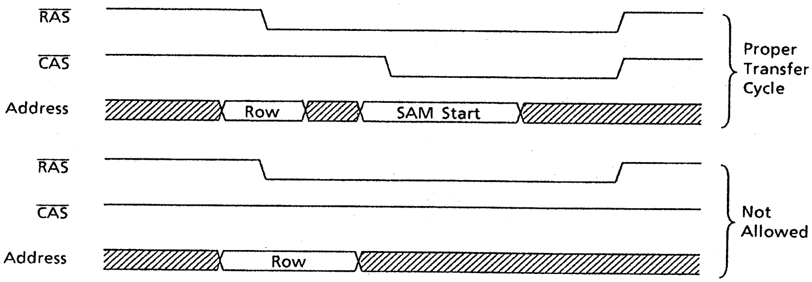


Figure 10. Example of SAM Register Operation Sequence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

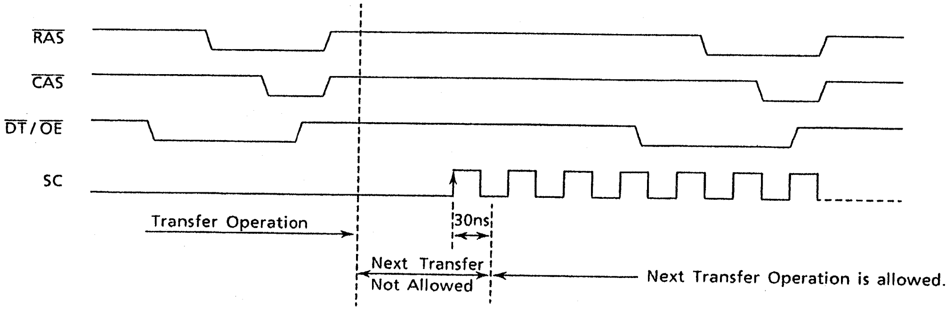
TRANSFER OPERATION WITHOUT $\overline{CAS}$

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column address are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore a transfer cycle with $\overline{CAS}$ held "high" is not allowed (Refer to the illustration below).



READ TRANSFER CYCLE AFTER READ TRANSFER CYCLE

Another read transfer may be performed following the read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC528126BJ/BZ/BFT/BTR is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μseconds pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
WM1 Register	Write Enable
TAP pointer	Invalid

TOSHIBA

DATA BOOK

MOS MEMORY
(VRAM, SRAM)

1991

INTRODUCTION

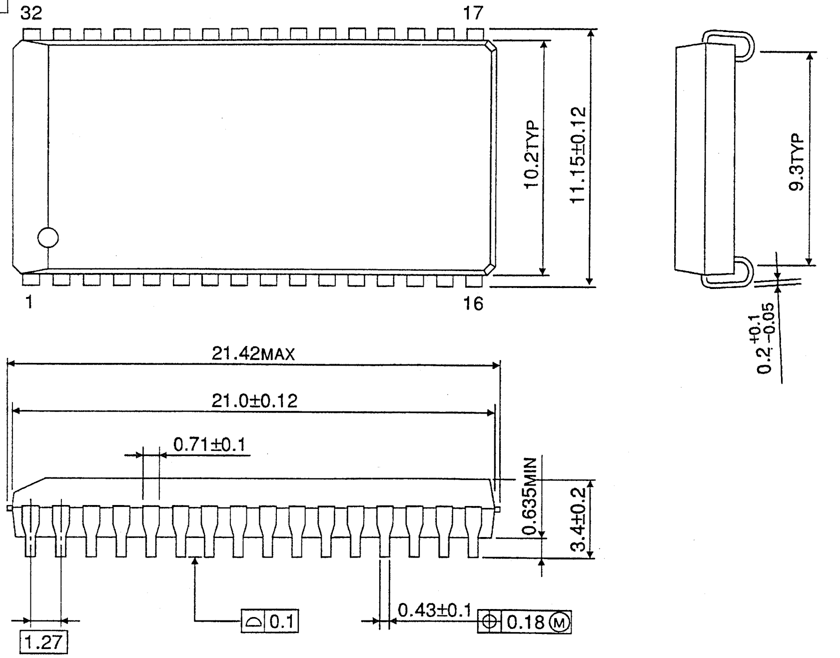
We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".
Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.
These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.
We hope this information will be very useful for you.

Nov. 1991

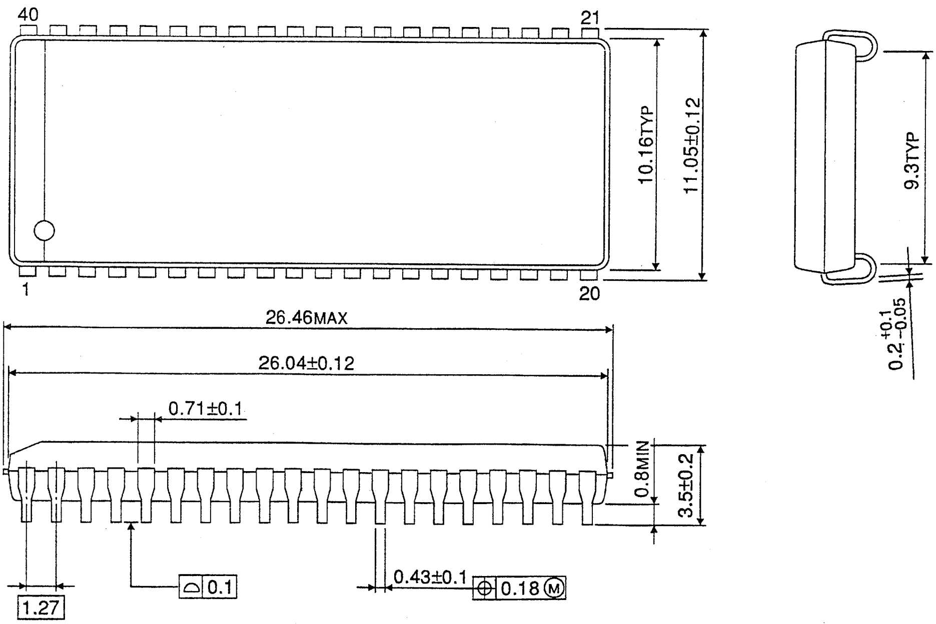
TOSHIBA CORPORATION
Semiconductor Group

Unit in mm

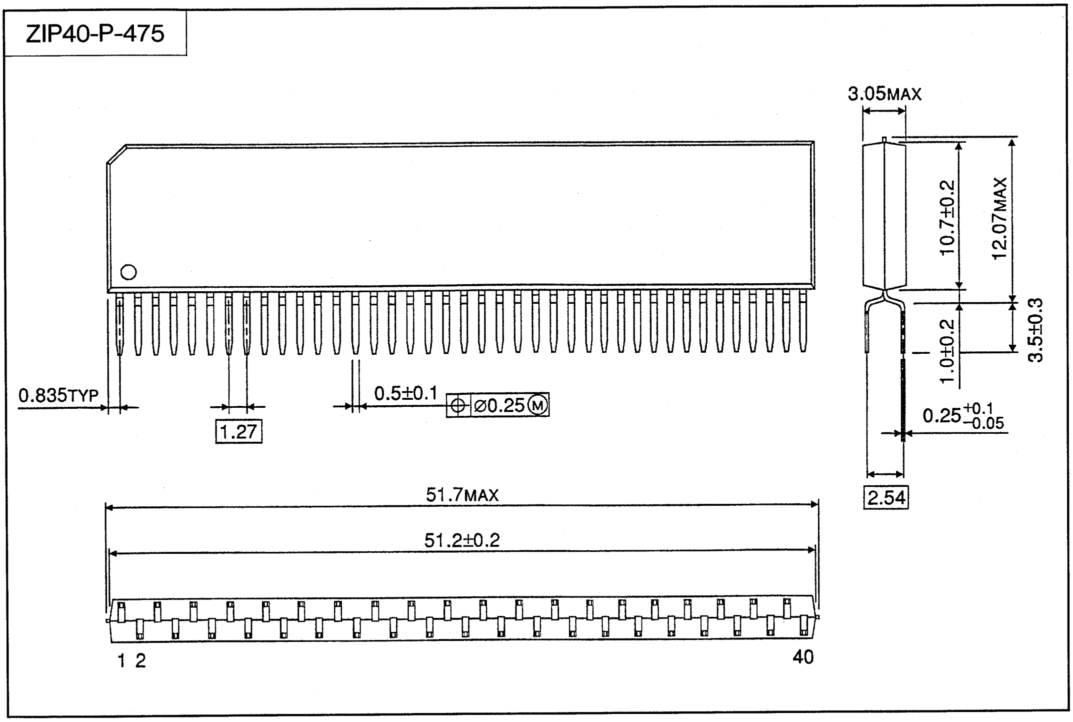
SOJ32-P-400A



SOJ40-P-400



Unit in mm

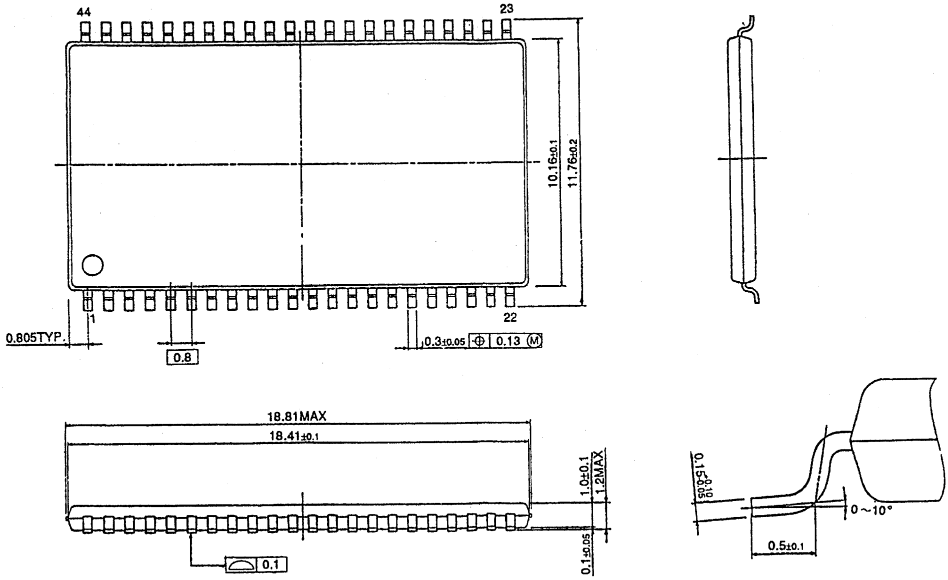


ZIP40-P-475
3.05MAX
10.7±0.2
12.07MAX
3.5±0.3
1.0±0.2
0.835TYP
1.27
0.5±0.1
Ø0.25 M
0.25 +0.1 −0.05
2.54
51.7MAX
51.2±0.2
1 2
40

Unit in mm

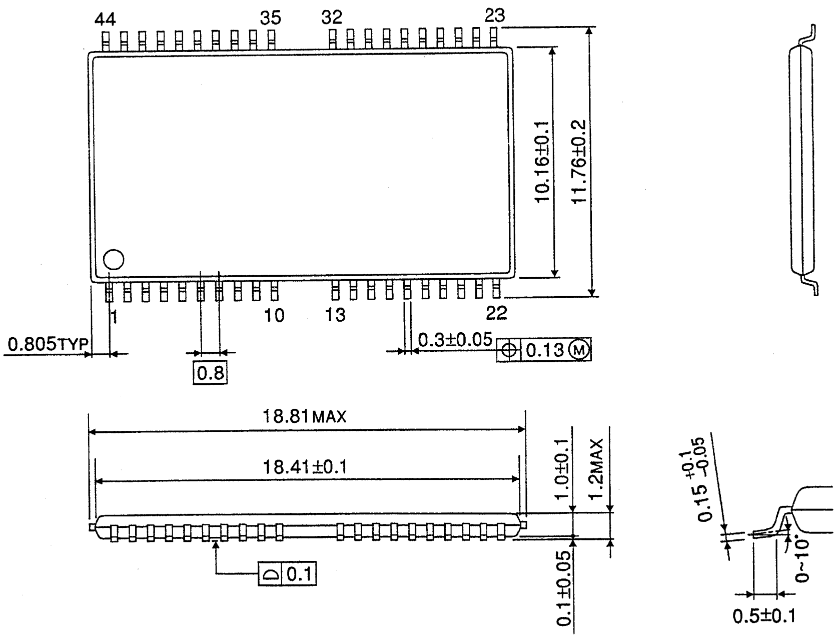
TSOP44-P-400

TENTATIVE

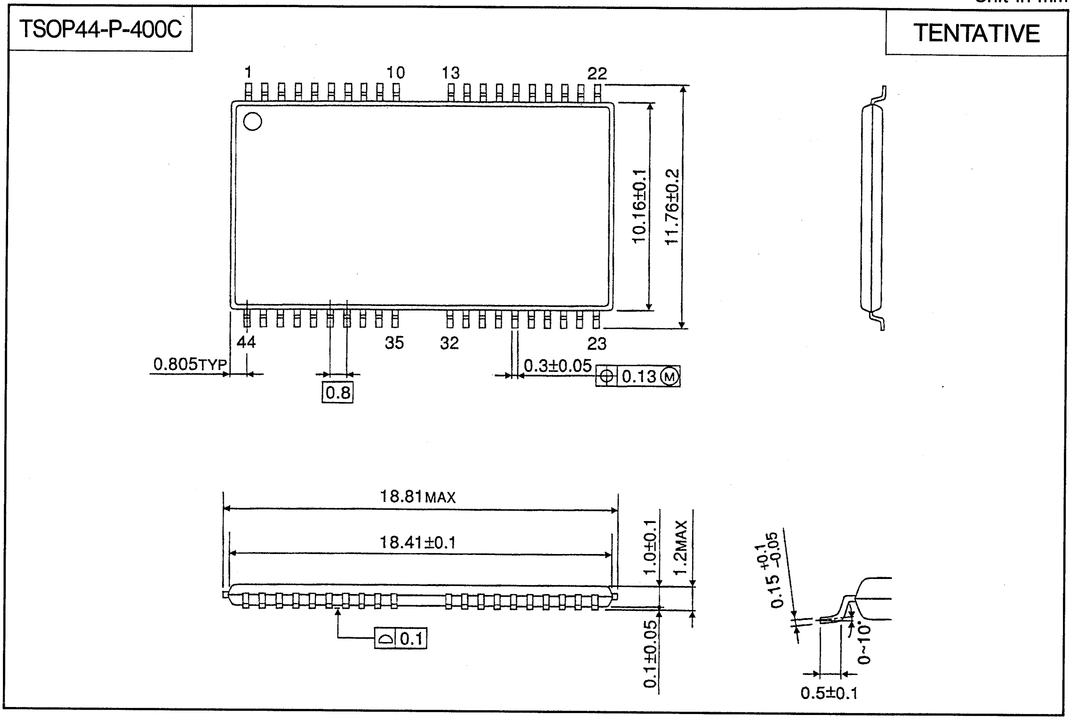


TSOP44-P-400B

TENTATIVE



Unit in mm



TSOP44-P-400C
TENTATIVE
1
10
13
22
44
35
32
23
10.16±0.1
11.76±0.2
0.805TYP
0.8
0.3±0.05
0.13 M
18.81MAX
18.41±0.1
1.0±0.1
1.2MAX
0.1
0.1±0.05
0.15 +0.1 -0.05
0~10°
0.5±0.1