

TC551001APL/AFL-70,-85,-10 TC551001AFTL/ATRL-70,-85,-10

TENTATIVE DATA

131,072 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC551001APL is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.) and minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in low power standby mode in which standby current is 2 μ A typically. The TC551001APL has three control inputs. Chip enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, and an output enable input (\overline{OE}) provides fast memory access. Thus the TC551001APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC551001APL is offered in a dual-in-line 32 pin standard plastic package, small-out-line plastic package and thin small-out-line plastic package (forward, reverse type).

FEATURES

- Low Power Dissipation
27.5mW / MHz (Typ.) Operating
- Standby Current: 100 μ A (Max.)
- 5V Single Power Supply
- Power Down Features : $\overline{CE1}$, CE2
- Data retention Supply Voltage: 2.0 ~ 5.5V
- Directly TTL Compatible
: All Inputs and Outputs

• Access Time (max.)

	TC551001APL/ AFL/AFTL/ATRL-70	TC551001APL/ AFL/AFTL/ATRL-85	TC551001APL/ AFL/AFTL/ATRL-10
Access Time	70ns	85ns	100ns
$\overline{CE1}$ Access Time	70ns	85ns	100ns
CE2 Access Time	70ns	85ns	100ns
\overline{OE} Access Time	35ns	45ns	50ns

- Package TC551001APL : DIP32-P-600
TC551001AFL : SOP32-P-525
TC551001AFTL : TSOP32-P-0820
TC551001ATRL : TSOP32-P-0820A

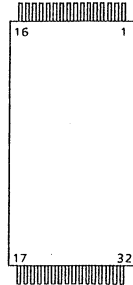
PIN CONNECTION (TOP VIEW)

o 32 PIN DIP & SOP

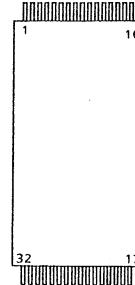
N.C.	1	32	V _{DD}
A16	2	31	A15
A14	3	30	CE2
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	\overline{OE}
A2	10	23	A10
A1	11	22	$\overline{CE1}$
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

o 32 PIN TSOP

(forward type)



(reverse type)



PIN NAMES

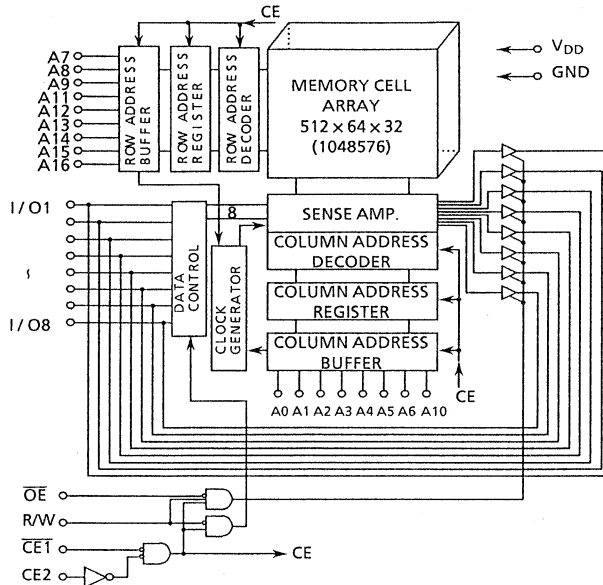
A0~A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Input
I/O1~I/O8	Data Input/Output
V _{DD}	Power (+ 5V)
GND	Ground
N.C.	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	N.C.	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A ₁₀	\overline{OE}

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BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	\overline{CET}	CE2	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D _{OUT}	I _{DDO}
Write	L	H	*	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	H	High-Z	I _{DDO}
Standby	H	*	*	*	High-Z	I _{DDs}
	*	L	*	*	High-Z	I _{DDs}

*: H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{solder}	Soldering Temperature	260 · 10	°C · sec
T _{strg.}	Storage Temperature	-55 ~ 150	°C
T _{opr.}	Operating Temperature	0 ~ 70	°C

*: -3.0V at pulse width 50ns MAX.

** : SOP

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D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP. 1	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.3	
V _{IL}	Input Low Voltage	-0.3	-	0.8	
V _{DH}	Data Retention Supply Voltage	2.0	-	5.5	

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70 °C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I _{IL}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}	-	-	± 1.0	μA	
I _{OH}	Output High Current	V _{OH} = 2.4V	-1.0	-	-	mA	
I _{OL}	Output Low Current	V _{OL} = 0.4V	4.0	-	-	mA	
I _{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or CE2 = V _{IL} or R/W = V _{IL} or $\overline{OE} = V_{IH}$, V _{OUT} = 0 ~ V _{DD}	-	-	± 1.0	μA	
I _{DDO1}	Operating Current	$\overline{CE1} = V_{IL}$ and CE2 = V _{IH} and R/W = V _{IH} , I _{OUT} = 0mA Other Inputs = V _{IH} / V _{IL}	Tcycle	Min.	-	70	mA
I _{DDO2}		$\overline{CE1} = 0.2V$ and CE2 = V _{DD} -0.2V R/W = V _{DD} -0.2V, I _{OUT} = 0mA Other Inputs = V _{DD} -0.2V/0.2V		Min.	-	60	
I _{DDO1}	Standby Current	$\overline{CE1} = V_{IH}$ or CE2 = V _{IL}	Tcycle	1 μs	-	-	20
I _{DDO2}		$\overline{CE1} = 0.2V$ and CE2 = V _{DD} -0.2V R/W = V _{DD} -0.2V, I _{OUT} = 0mA Other Inputs = V _{DD} -0.2V/0.2V		1 μs	-	-	10
I _{DDS1}	Standby Current	$\overline{CE1} = V_{IH}$ or CE2 = V _{IL}	Tcycle	-	-	3	mA
I _{DDS2} (1)		$\overline{CE1} = V_{DD} - 0.2V$ or CE2 = 0.2V V _{DD} = 2.0V ~ 5.5V, Ta = 0 ~ 70°C		-	2	100	μA

Note: (1) In standby mode with $\overline{CE1} \geq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of CE2 $\geq V_{DD} - 0.2V$ or CE2 $\leq 0.2V$.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	

Note: This parameter periodically sampled is not 100% tested.

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A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC551001APL-70 TC551001AFL-70 TC551001AFTL-70 TC551001ATRL-70		TC551001APL-85 TC551001AFL-85 TC551001AFTL-85 TC551001ATRL-85		TC551001APL-10 TC551001AFL-10 TC551001AFTL-10 TC551001ATRL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	–	85	–	100	–	ns
t _{ACC}	Address Access Time	–	70	–	85	–	100	
t _{CO1}	$\overline{CE1}$ Access Time	–	70	–	85	–	100	
t _{CO2}	CE2 Access Time	–	70	–	85	–	100	
t _{OE}	Output Enable to Output in Valid	–	35	–	45	–	50	
t _{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	–	10	–	10	–	
t _{OEE}	Output Enable to Output in Low-Z	5	–	5	–	5	–	
t _{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	25	–	30	–	35	
t _{ODO}	Output Enable to Output in High-Z	–	25	–	30	–	35	
t _{OH}	Output Data Hold Time	10	–	10	–	10	–	

WRITE CYCLE

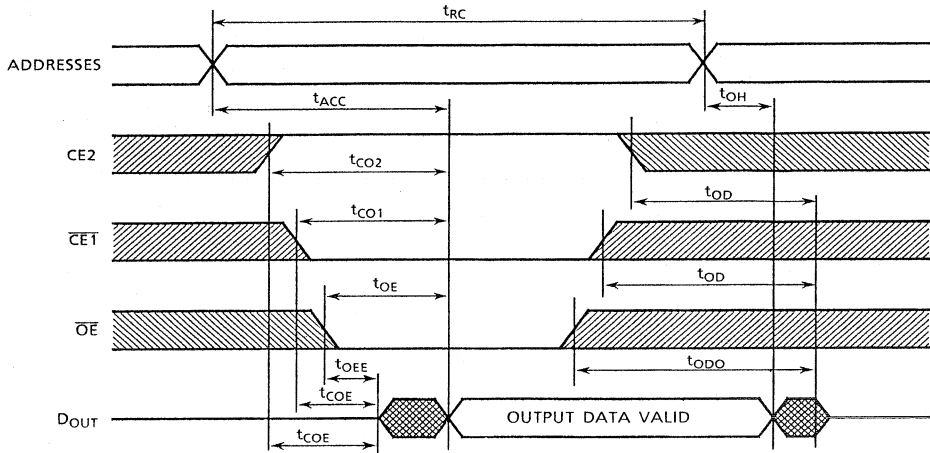
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		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	–	85	–	100	–	ns
t _{WP}	Write Pulse Width	50	–	60	–	60	–	
t _{CW}	Chip Selection to End of Write	60	–	75	–	80	–	
t _{AS}	Address Set up Time	0	–	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	0	–	
t _{ODW}	R/W to Output in High-Z	–	25	–	30	–	35	
t _{OEW}	R/W to Output in Low-Z	5	–	5	–	5	–	
t _{DS}	Data Set up Time	30	–	35	–	40	–	
t _{DH}	Data Hold Time	0	–	0	–	0	–	

A.C. TEST CONDITIONS

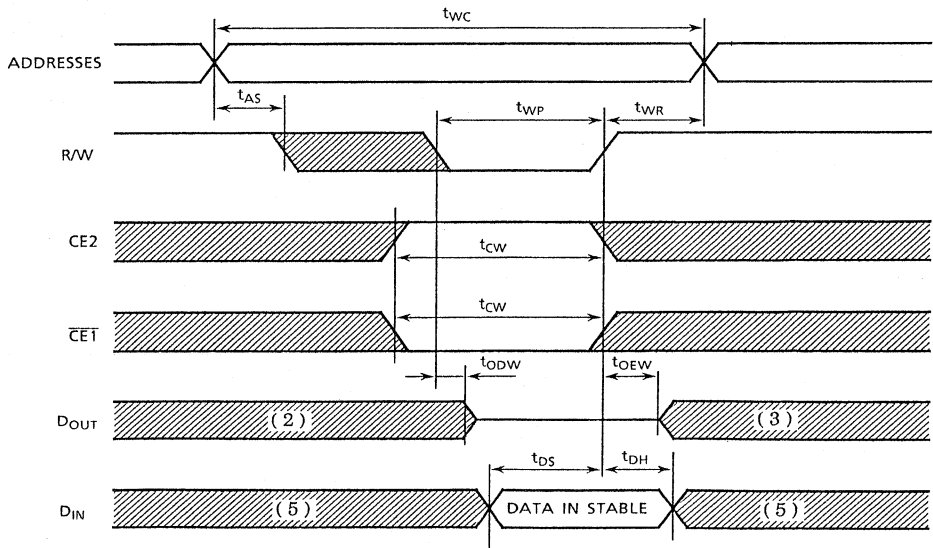
- Output Load : 100pF+1 TTL Gate
- Input Pulse Level : 0.6V, 2.4V
- Timing Measurement V_{IN} : 1.5V
Reference Level V_{OUT} : 1.5V
- t_r, t_f : 5ns

TIMING WAVEFORMS

READ CYCLE 1 (1)

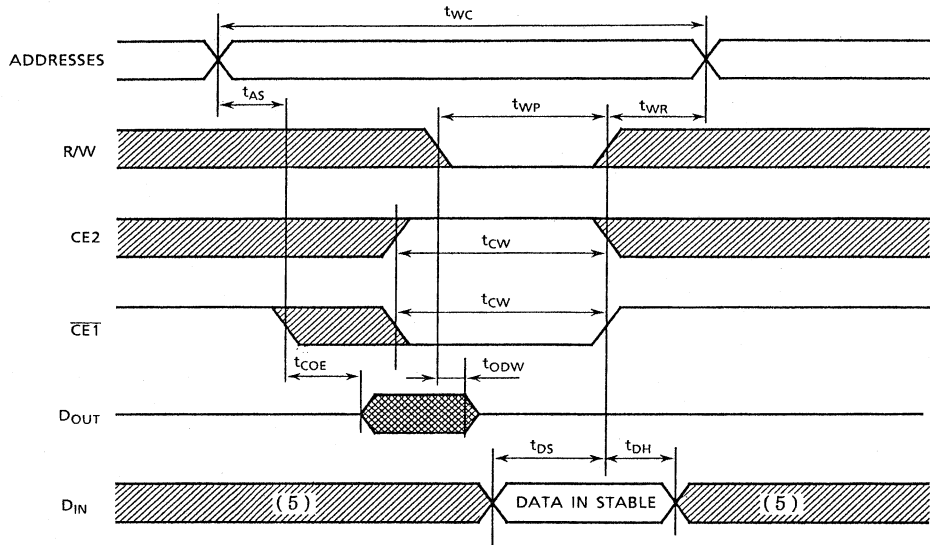


WRITE CYCLE 1 (4) (R/W Controlled Write)

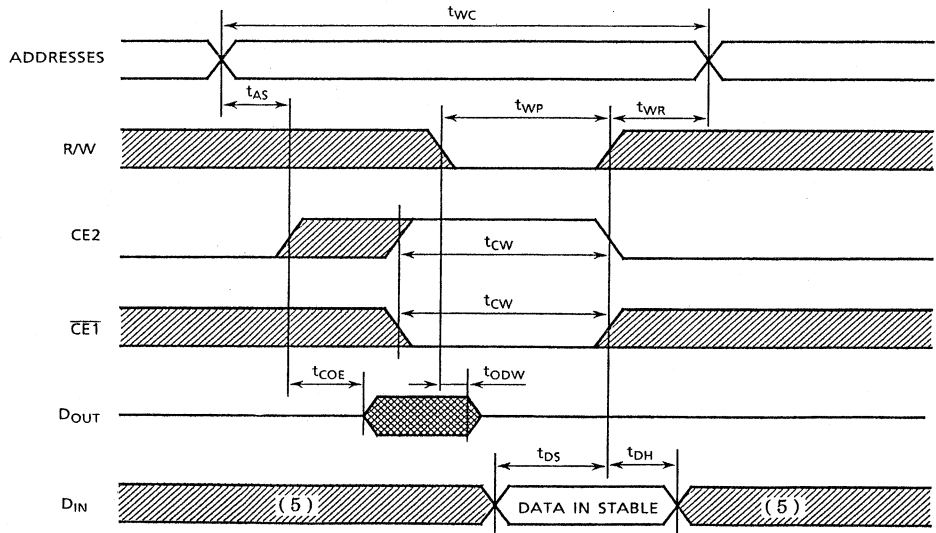


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WRITE CYCLE 2 (4) ($\overline{\text{CE1}}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



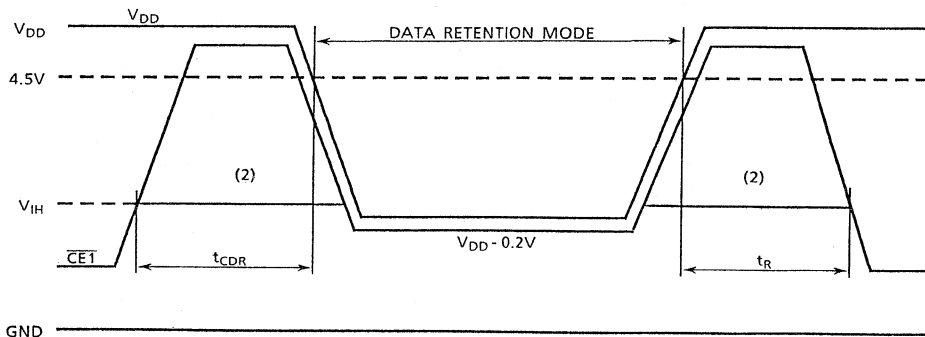
NOTE:

- (1) R/W is High for Read Cycle.
- (2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
- (3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.
- (4) Assuming that \overline{OE} is High for Write Cycle, Outputs are in high impedance state during this period.
- (5) The I/O may be in the output state at this time, input signals of opposite phase must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

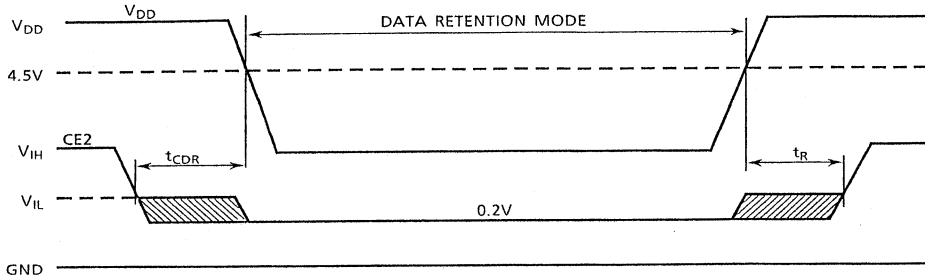
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V
I_{DSS2}	Standby Current	$V_{DD} = 3.0V$	-	50	μA
		$V_{DD} = 5.5V$	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode	0	-	-	nS
t_R	Recovery Time	5	-	-	mS

CE1 Controlled Data Retention Mode (1)



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CE2 Controlled Data Retention Mode (3)



NOTE:

- (1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE2 \leq 0.2V$ or $CE2 \geq V_{DD} - 0.2V$.
- (2) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDSI} current flows.
- (3) In $CE2$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE2 \leq 0.2V$.

TOSHIBA

DATA BOOK

MOS MEMORY
(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

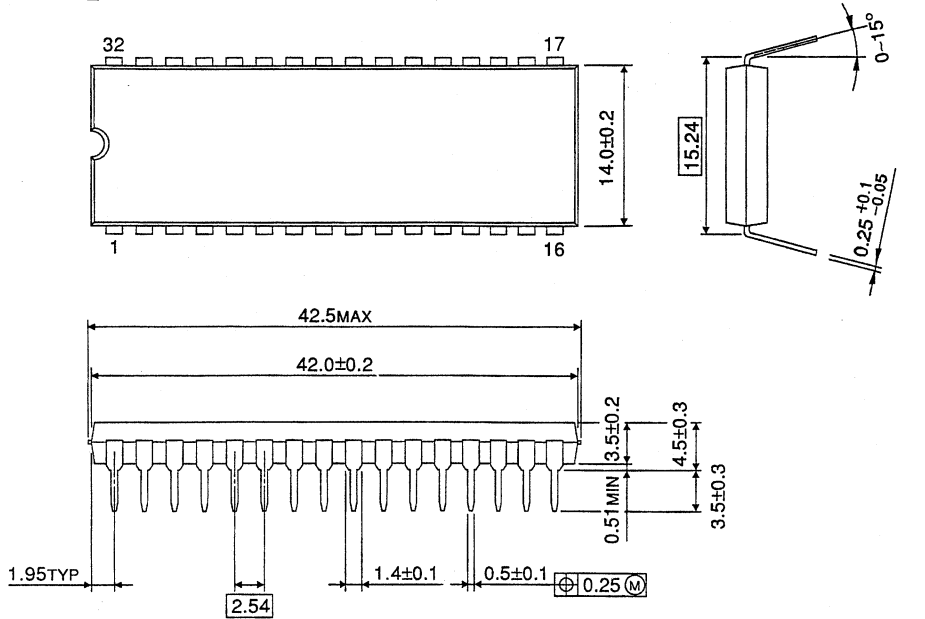
These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

We hope this information will be very useful for you.

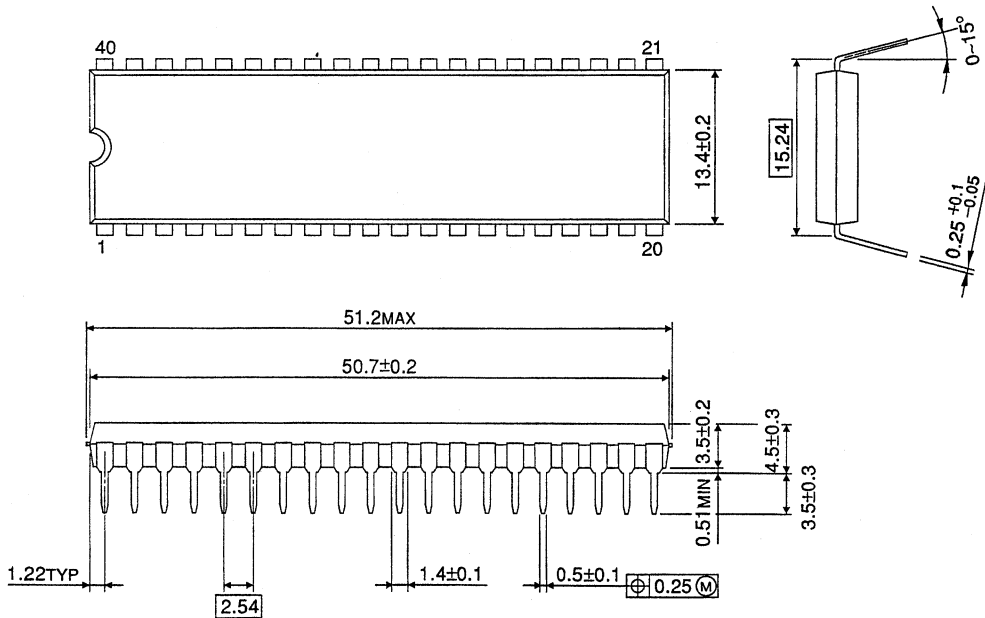
Nov. 1991

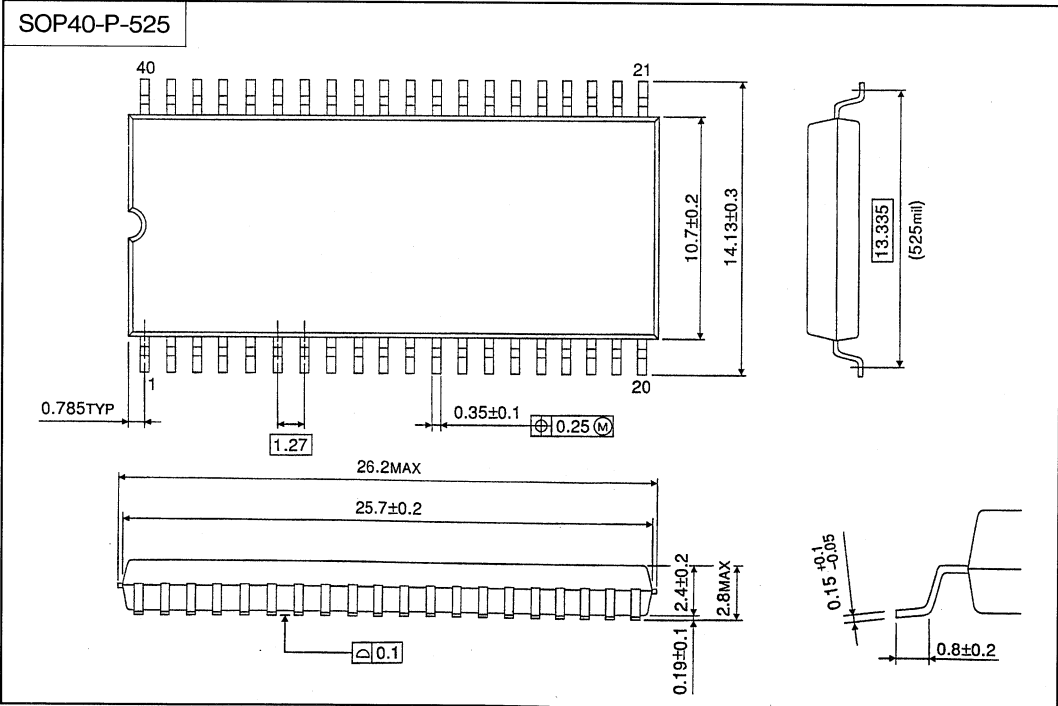
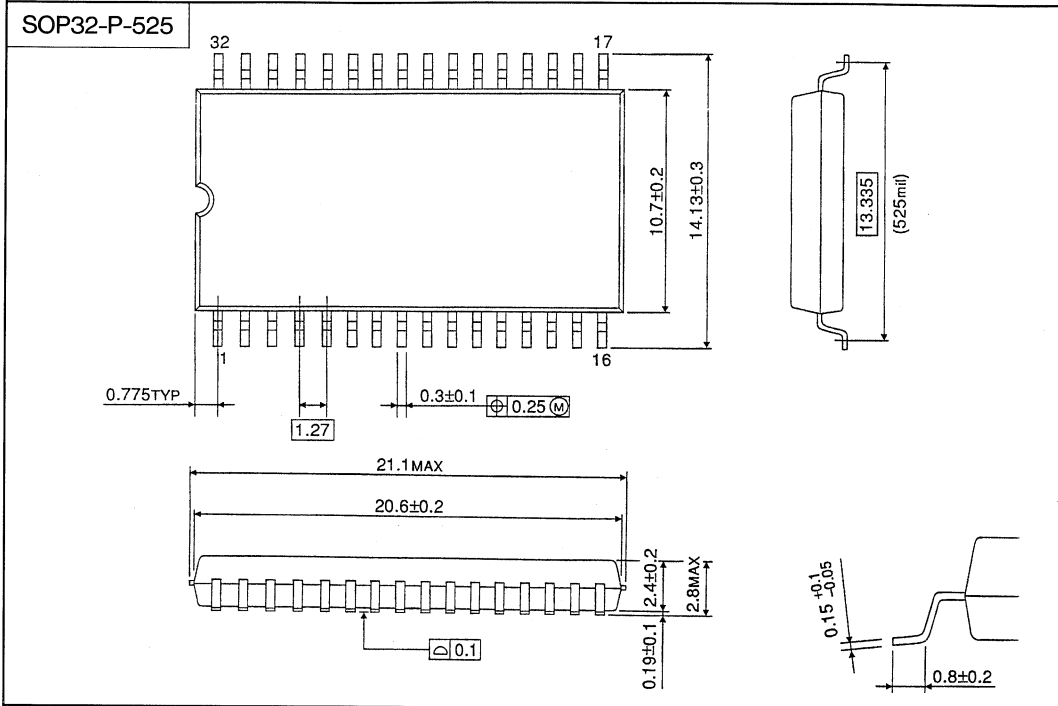
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Semiconductor Group

DIP32-P-600



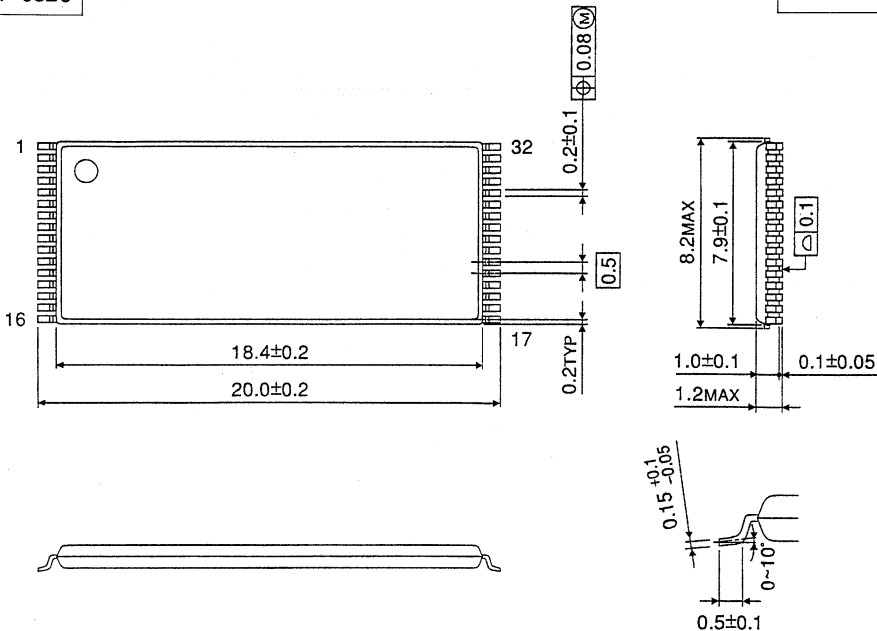
DIP40-P-600





TSOP32-P-0820

TENTATIVE



TSOP32-P-0820A

TENTATIVE

