TC551001PL/FL-85, -10

131,072 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC551001PL/FL is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5 V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5 mA/MHz (Typ.) and minimum cycle time of 85/100 ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in low power standby mode in which standby current is 2 μA typically. The TC551001PL/FL has three control inputs. Chip enable inputs ($\overline{CE1}$,CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC551001PL/FL is suitable for use in various microprocessor application system where high speed, low power, and battery back up are required.

The TC551001PL/FL is offered in both a dual-in-line 32 pin standard plastic package and small-out line plastic flat package.

FEATURES

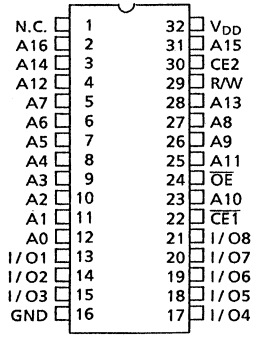
- Low Power Dissipation
  : 27.5 mW/MHz (Typ.)
- Standby Current : 100 μA (Max.)
- 5 V Single Power Supply
- Power Down Feature : $\overline{CE1}$, CE2
- Data retention Supply Voltage : 2.0 ~ 5.5 V
- Directly TTL Compatible
  : All Inputs and Outputs

- Access Time

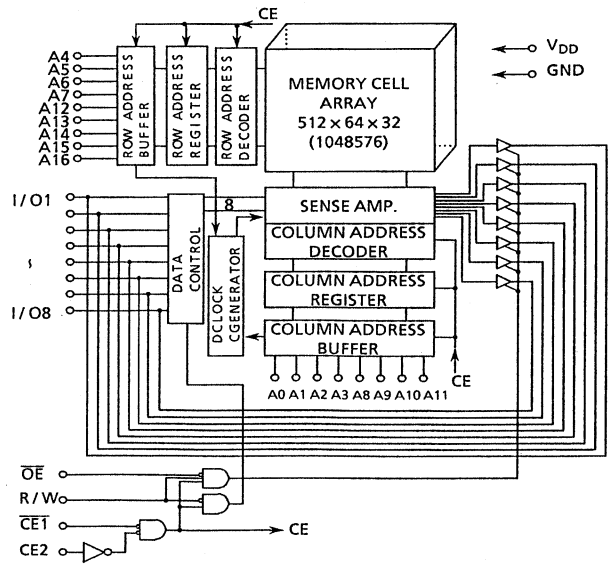
	TC551001 PL/FL-85	TC551001 PL/FL-10
Access Time (max.)	85 ns	100 ns
$\overline{CE1}$ Access Time (max.)	85 ns	100 ns
CE2 Access Time (max.)	85 ns	100 ns
$\overline{OE}$ Access Time (max.)	45 ns	50 ns

- Package : TC551001PL : DIP32-P-600
  TC551001FL : SOP32-P-525

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$,CE2	Chip Enable Input
I/O1~I/O8	Data Input/Output
V_{DD}	Power (+5 V)
GND	Ground
N.C.	No Connection

OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	− 0.3 ~ 7.0	V
V_{IN}	Input Voltage	− 0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	− 0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0 / 0.6**	W
Tsolder	Soldering Temperature	260 · 10	°C · sec
Tstrg.	Storage Temperature	− 55 ~ 150	°C
Topr.	Operating Temperature	0 ~ 70	°C

* : −3.0 V at pulse width 50 ns MAX. ** : SOP

D.C. RECOMMENDED OPERATING CONDITIONS.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	− 0.3	−	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70\,°C$, $V_{DD} = 5\,V \pm 10\,\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	–	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\,V$	– 1.0	–	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\,V$	4.0	–	–	mA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	–	–	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ and $R/W = V_{IH}$, $I_{OUT} = 0\,mA$, Other Inputs = V_{IH}/V_{IL}, t_{cycle} = Min. cycle	–	–	80	mA
I_{DDO2}		$\overline{CE1} = 0.2\,V$ and $CE2 = V_{DD} - 0.2\,V$, $R/W = V_{DD} - 0.2\,V$, $I_{OUT} = 0\,mA$, Other Inputs = $V_{DD} - 0.2\,V / 0.2\,V$, t_{cycle} = Min. cycle	–	–	70	mA
I_{DDS1}	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$	–	–	3	mA
I_{DDS2} (1)		$\overline{CE1} = V_{DD} - 0.2\,V$ or $CE2 = 0.2\,V$, $V_{DD} = 2.0\,V \sim 5.5\,V$, $Ta = 0 \sim 70\,°C$	–	2	100	μA

Note : (1) In standby mode with $\overline{CE1} \geqq V_{DD} - 0.2\,V$, these specification limits are guaranteed under the condition of $CE2 \geqq V_{DD} - 0.2\,V$ or $CE2 \leqq 0.2\,V$.

CAPACITANCE ($Ta = 25\,°C$, $f = 1\,MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note : This parameter periodically sampled is not 100 % tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70 °C, V_{DD} = 5 V ± 10 %)

Read Cycle

SYMBOL	PARAMETER	TC551001PL-85 TC551001FL-85		TC551001PL-10 TC551001FL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO1}	$\overline{CE1}$ Access Time	–	85	–	100	
t_{CO2}	CE2 Access Time	–	85	–	100	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	0	–	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	30	–	35	
t_{ODO}	Output Enable to Output in High-Z	–	30	–	35	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

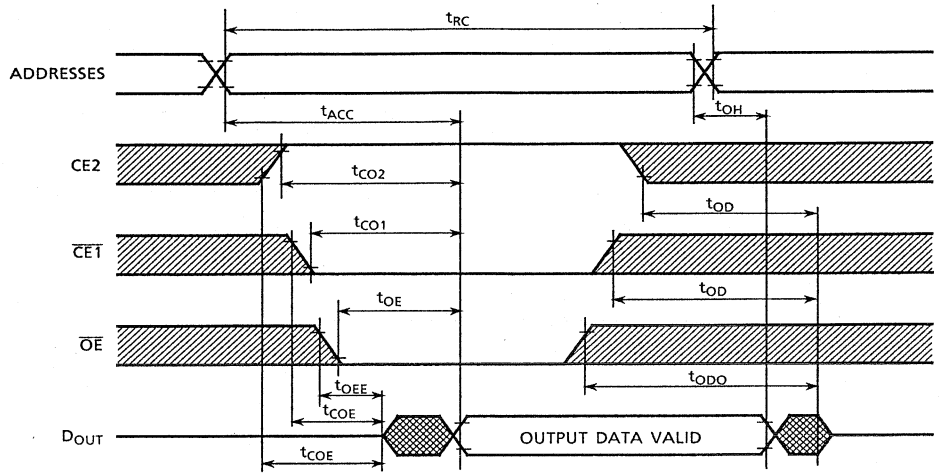
SYMBOL	PARAMETER	TC551001PL-85 TC551001FL-85		TC551001PL-10 TC551001FL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	60	–	60	–	
t_{CW}	Chip Selection to End of Write	75	–	80	–	
t_{AS}	Address Set up Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	30	–	35	
t_{OEW}	R/W to Output in Low-Z	0	–	0	–	
t_{DS}	Data Set up Time	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

A.C. TEST CONDITIONS

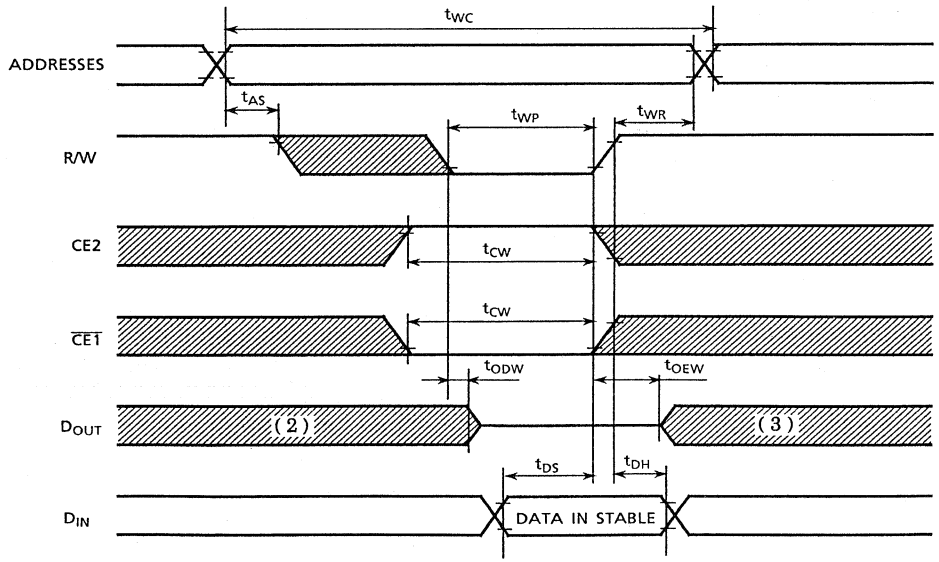
Output Load	:	100 pF + 1 TTL Gate
Input Pulse Level	:	0.6 V, 2.4 V
Timing Measurement V_{IN}	:	0.8 V, 2.2 V
Reference Level V_{OUT}	:	0.8 V, 2.2 V
t_r, t_f	:	5 ns

TIMING WAVEFROMS

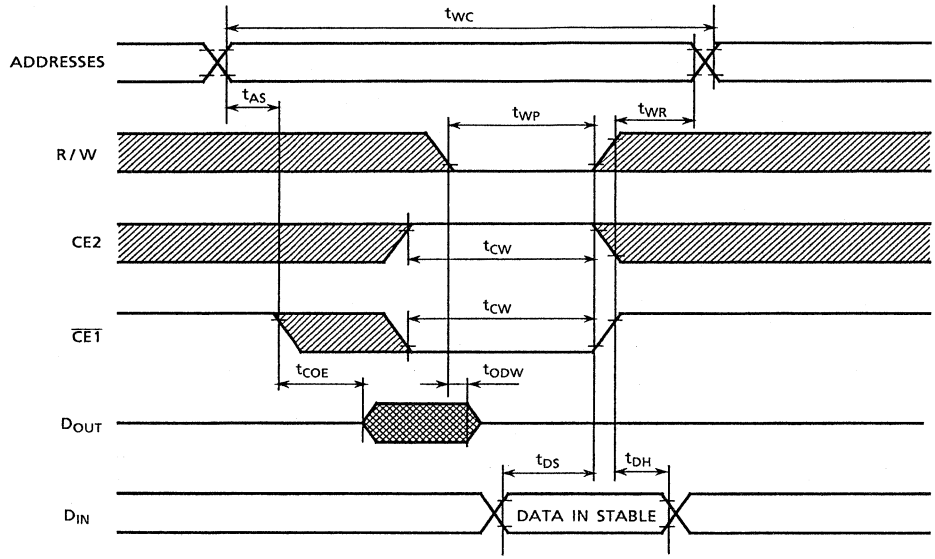
Read Cycle (1)



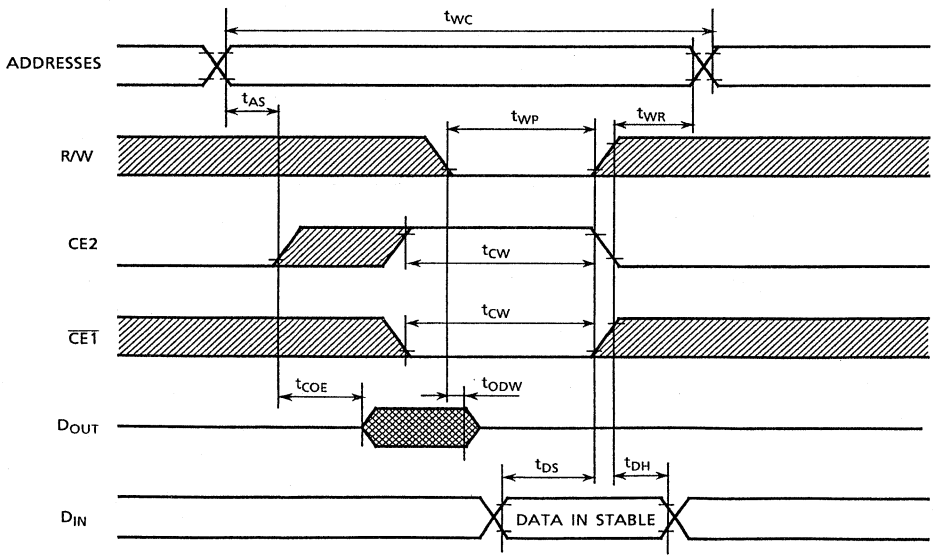
Write Cycle 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



Note : (1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

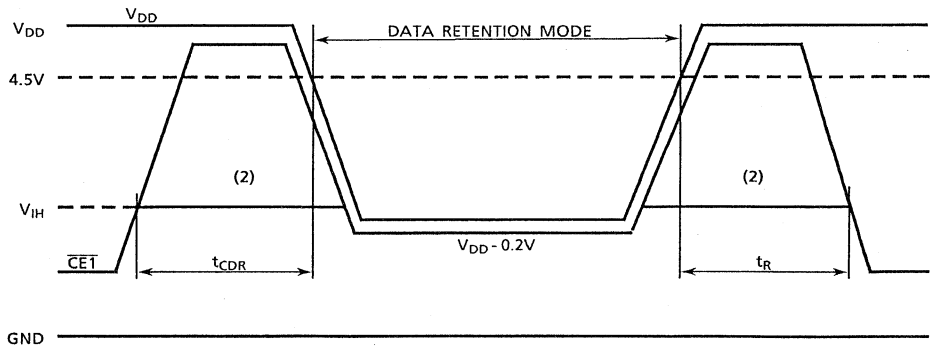
(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

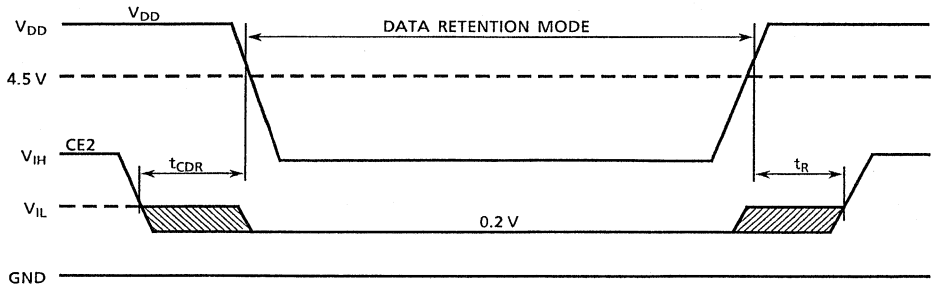
DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0 V	–	–	50	μA
		V_{DD} = 5.5 V	–	–	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	–	–	nS
t_R	Recovery Time		5	–	–	mS

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Note : (1) In $\overline{CE1}$ controlled data retention mode, minmum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2 V or CE2 $\geqq$ V_{DD} − 0.2 V.

(2) If the V_{IH} of $\overline{CE1}$ is 2.2 V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4 V, I_{DDS1} current flows.

(3) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2 V.

TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

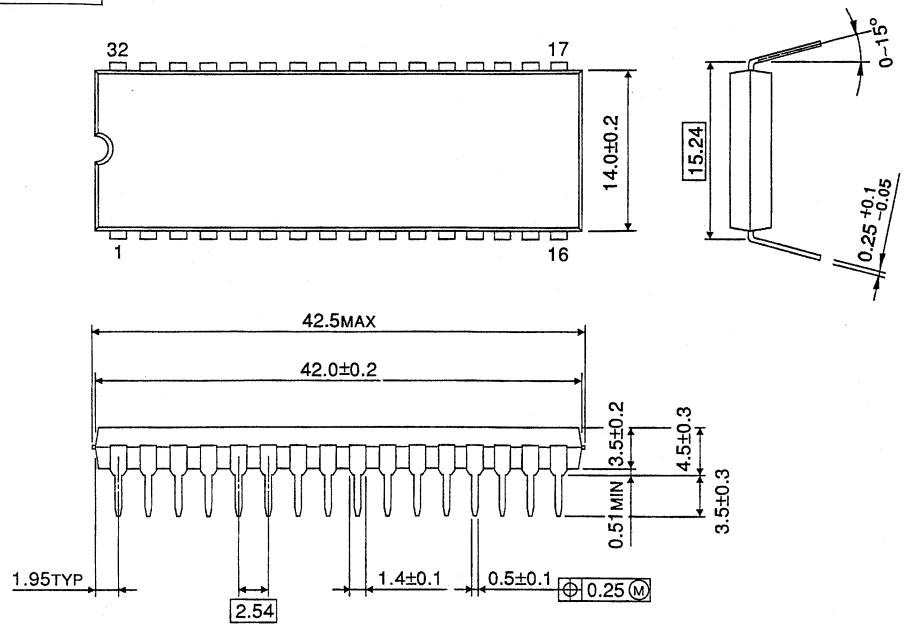
We hope this information will be very useful for you.

Nov. 1991

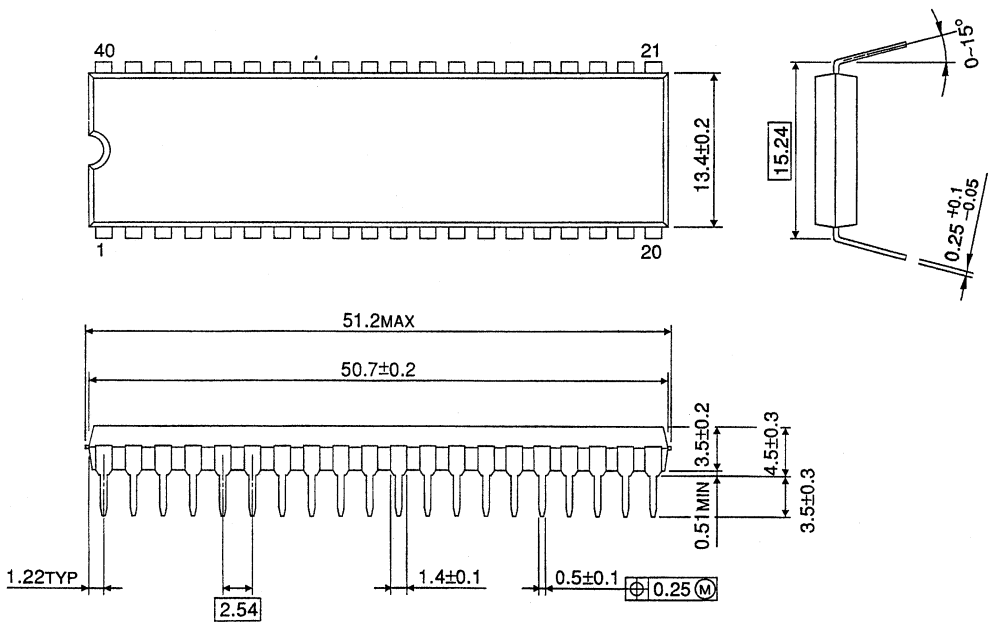
TOSHIBA CORPORATION
Semiconductor Group

Unit in mm

DIP32-P-600

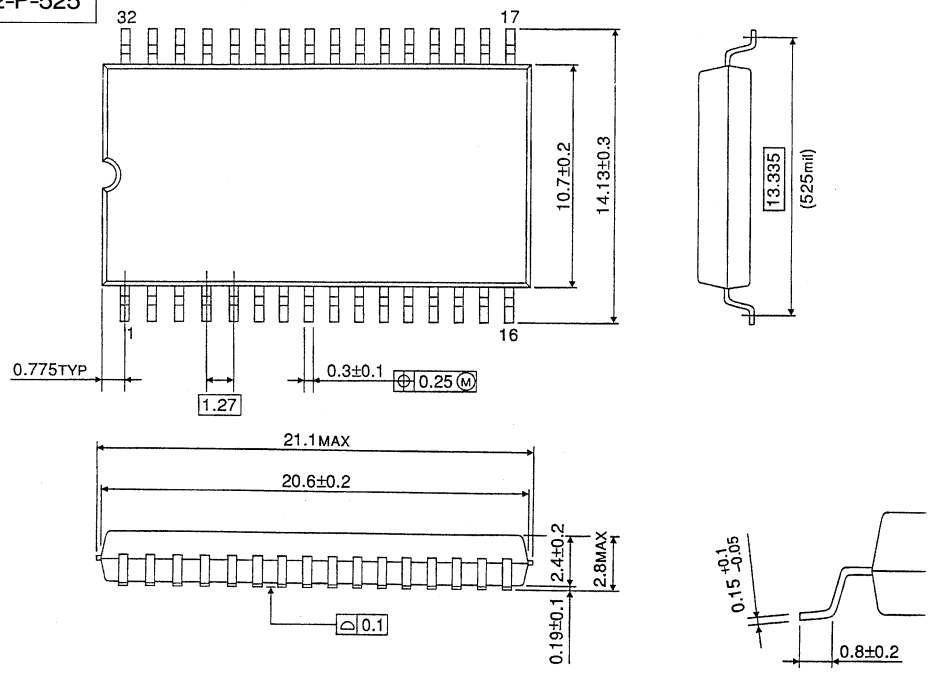


DIP40-P-600



Unit in mm

SOP32-P-525



SOP40-P-525