TC551664J-15,-20,-25

65,536 WORD × 16 BIT CMOS STATIC RAM

DESCRIPTION

The TC551664J is a 1,048,576 bits high speed static random access memory organized as 65,536 words by 16 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC551664J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access. Also it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC551664J is suitable for use in various application systems where high speed is required as cache memory, high speed strage, and so on. All Inputs and Outputs are directly TTL compatible.

The TC551664J is moulded in 44 pin plastic SOJ with 400 mil width for high density surface assembly.

FEATURES

- Fast access time :

TC551664J-15	15ns (MAX.)
TC551664J-20	20ns (MAX.)
TC551664J-25	25ns (MAX.)

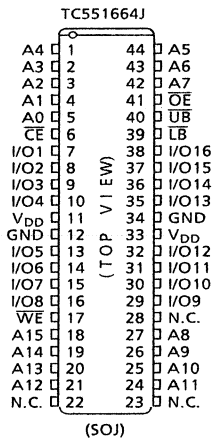
- Low power dissipation

Cycle Time	15	20	25	30	50	ns
Operation (MAX.)	260	220	200	180	150	mA

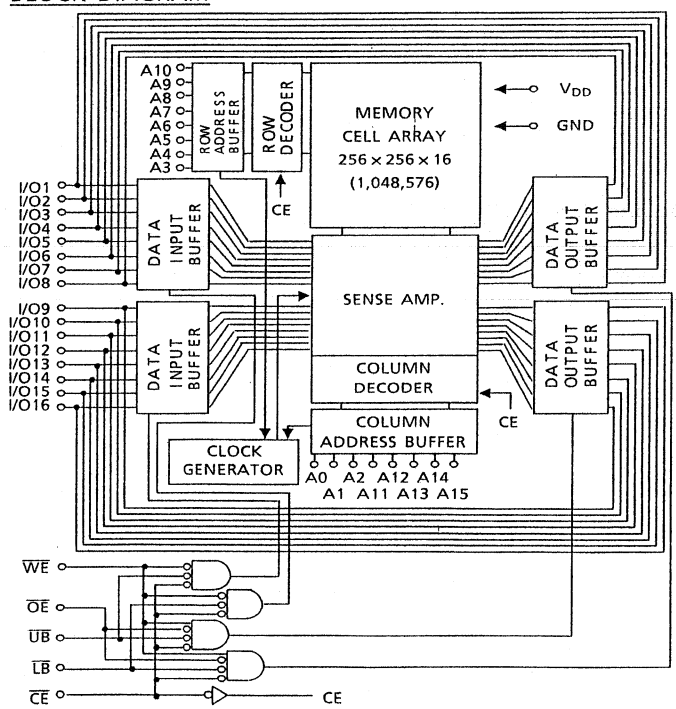
Standby : 1mA (MAX.)

- 5V single power supply : 5V ± 10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Data byte control
  $\overline{LB}$ (I/O1~I/O8), $\overline{UB}$ (I/O9~I/O16)
- Package : SOJ44-P-400

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A15	Address Inputs
I/O1~I/O16	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power(+5V)
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Terminal Voltage	−2.0 * ~7.0	V
$V_{I/O}$	Input / Output Terminal Voltage	−0.5 * ~VDD + 0.5	V
P_D	Power Dissipation	1.5	W
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

* : −3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Suply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	−0.5 *	−	0.8	V

* : −3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		−	−	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0~VDD		−	−	± 10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	−	−	mA
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, Iout = 0mA Other Inputs = V_{IH} / V_{IL}	tcycle = 15ns	−	−	260	mA
			tcycle = 20ns	−	−	220	
			tcycle = 25ns	−	−	200	
			tcycle = 30ns	−	−	180	
			tcycle = 50ns	−	−	150	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH} / V_{IL}		−	−	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Inputs = V_{DD} − 0.2V or 0.2V		−	−	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

* : H or L

AC CHARACTERISTICS (Ta = 0~70°C [1], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC551664J - 15		TC551664J - 20		TC551664J - 25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	
t_{CO}	$\overline{CE}$ Access Time	–	15	–	20	–	25	
t_{OE}	$\overline{OE}$ Access Time	–	8	–	10	–	12	
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	–	8	–	10	–	12	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	1	–	
t_{BE}	Output Enable Time from $\overline{UB}$, $\overline{LB}$	1	–	1	–	1	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	8	–	8	–	8	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	–	8	
t_{BD}	Output Disable Time from $\overline{UB}$, $\overline{LB}$	–	8	–	8	–	8	

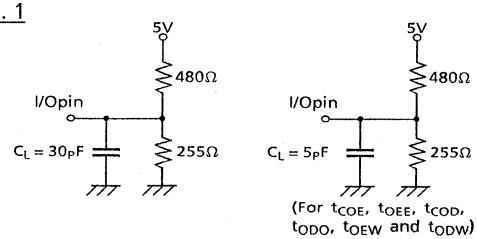
WRITE CYCLE

SYMBOL	PARAMETER	TC551664J - 15		TC551664J - 20		TC551664J - 25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	ns
t_{WP}	Write Pulse Width	9	–	10	–	12	–	
t_{CW}	Chip Enable to End of Write	12	–	13	–	15	–	
t_{BW}	$\overline{UB}$, $\overline{LB}$ Enable to End of Write	9	–	12	–	14	–	
t_{AW}	Address Valid to End of Write	9	–	12	–	14	–	
t_{AS}	Address Set Up Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{DS}	Data Set Up Time	8	–	10	–	10	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	–	8	

AC TEST CONDITIONS

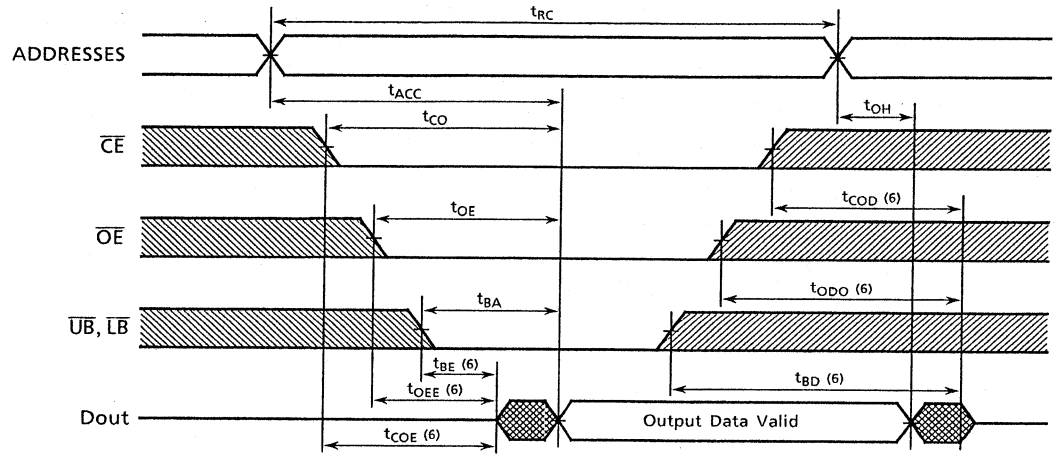
Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

FIG. 1

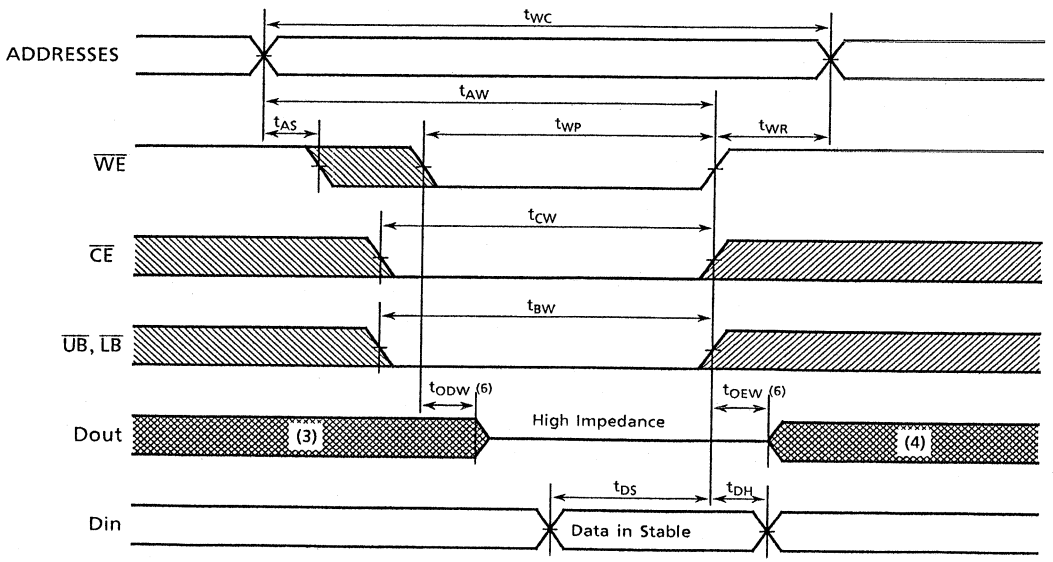


TIMING WAVEFORMS

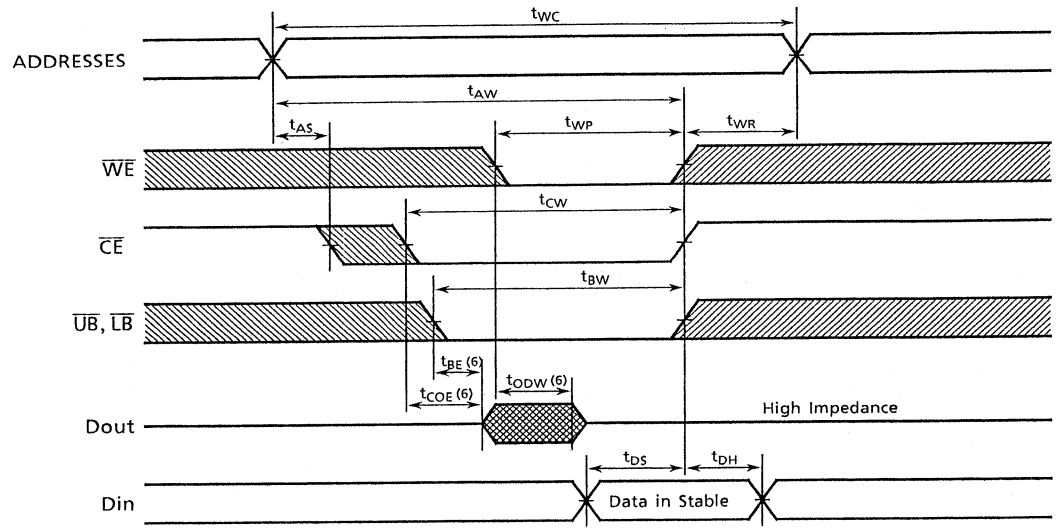
READ CYCLE (2)



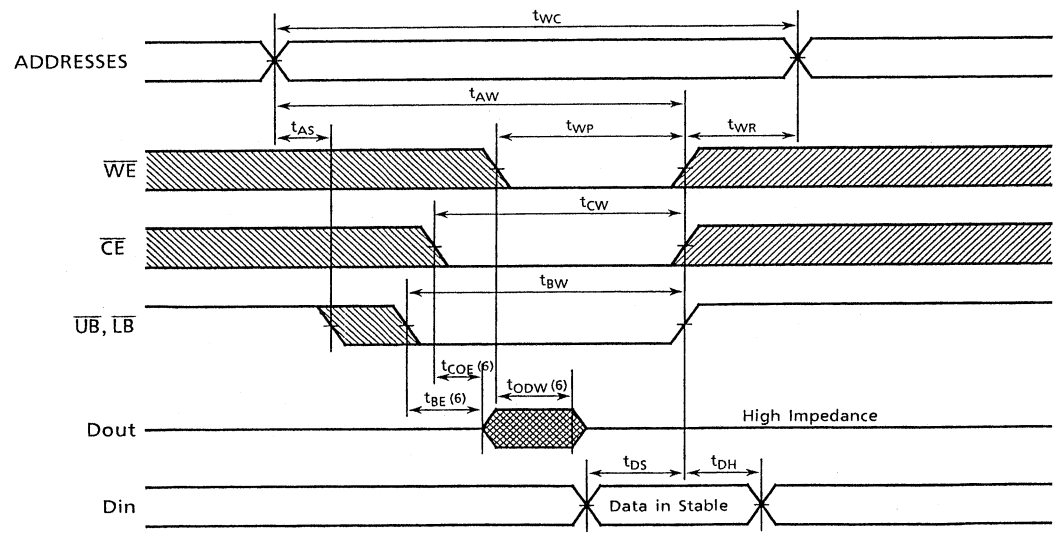
WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled)



WRITE CYCLE 2 (5) ($\overline{CE}$ Controlled)



WRITE CYCLE 3 (5) ($\overline{UB}$, $\overline{LB}$ Controlled)

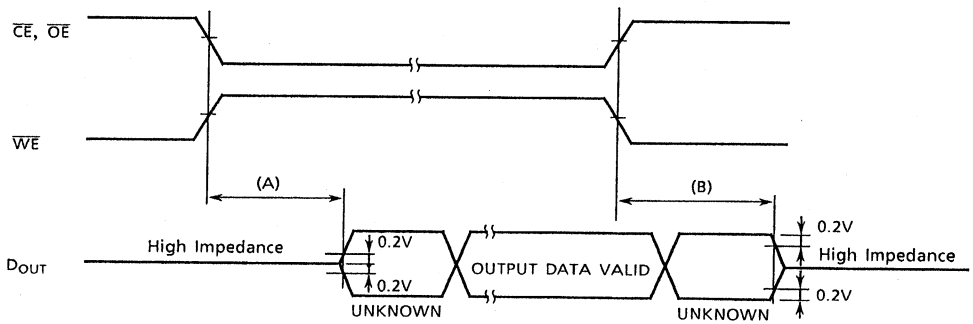


NOTE :

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. $\overline{WE}$ is High for Read Cycle.
3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior $\overline{WE}$ High transition, Outputs remain in a high impedance state.
5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.
6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEE}, t_{BE}, t_{OEW} ····· Output Enable Time

   (B) t_{COD}, t_{ODO}, t_{BD}, t_{ODW} ····· Output Disable Time



TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

We hope this information will be very useful for you.

Nov. 1991

TOSHIBA CORPORATION
Semiconductor Group

Unit in mm

SOJ44-P-400