SILICON GATE CMOS DIGITAL INTEGRATED CIRCUIT

TC55187T-20,-25,-35

2-WAY 4,096 WORDS × 18 BITS / 8,192 WORDS × 18 BITS
CMOS STATIC CACHE DATA RAM

DESCRIPTION

The TC55187T is a 147,456 bits high-speed static RAM which can be user-configured either as 2-way 4,096 words by 18 bits or as 8,192 words by 18 bits. It is provided with a byte control and on-chip address latches. The TC55187T is fabricated using Toshiba's CMOS technology and advanced circuit techniques which provide the high speed feature, and is operated from a single 5-volt supply. This device features address access time as fast as 20ns, output-enable access as fast as 10ns and simple interfacing capability with bipolar TTL circuits. The TC55187T can directly interface with the INTEL 82385 cache controller, without requiring additional peripheral circuit such as latches, transceivers and gates. Therefore ; Significant reductions in the number of parts, board assembly area and power dissipation can be achieved by using the TC55187T cache data RAM. The MODE input of the TC55187T allows the user to configure the memory internally either as a 2-way 4,096 words by 18 bits organization which is suitable for 2-way set associative cache designs or as a 8,192 words by 18 bits organization suitable for direct map cache designs. The TC55187T can also be operated as a conventional asynchronous static RAM, which can be accessed from change of address, by holding the ALE input in the high state. The TC55187T is packaged in a 52-pin standard PLCC for high-density board level assembly.

FEATURES

- Fast Access Time (max.)

ITEM		TC55187T		
		-20	-25	-30
t_{RC}	Cycle Time	20ns	25ns	30ns
t_{AA}	Address Access Time	20ns	25ns	30ns
t_{OE}	$\overline{OE}$ Access Time	10ns	10ns	12ns

- Power dissipation

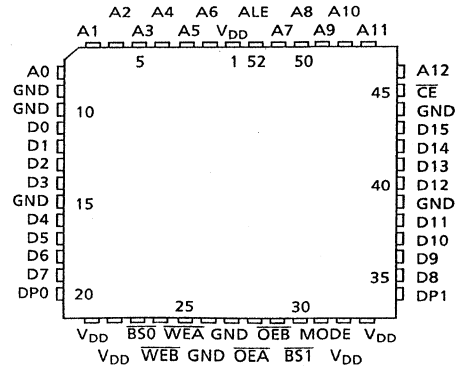
Operating	TC55187T-20	230mA (max.)
	TC55187T-25	220mA (max.)
	TC55187T-30	200mA (max.)
Standby		40mA (max.)

- Configurable for 2-way or direct RAM arrays
  2-way 4,096words×18bits (MODE = V_{IH})
  8,192words×18bits (MODE = V_{IL})
- Contains address latches (except A12) and byte control, $\overline{BS0}$ and $\overline{BS1}$
- Interfaces directly with the Intel 82385 Cache Controller
- Single power supply of 5V ± 10%
- All inputs and outputs TTL compatible
- Two Output buffer controls : $\overline{OEA}$, $\overline{OEB}$
- Two Write enable controls : $\overline{WEA}$, $\overline{WEB}$
- TC55187T : QFJ52-P-S750

PIN NAMES

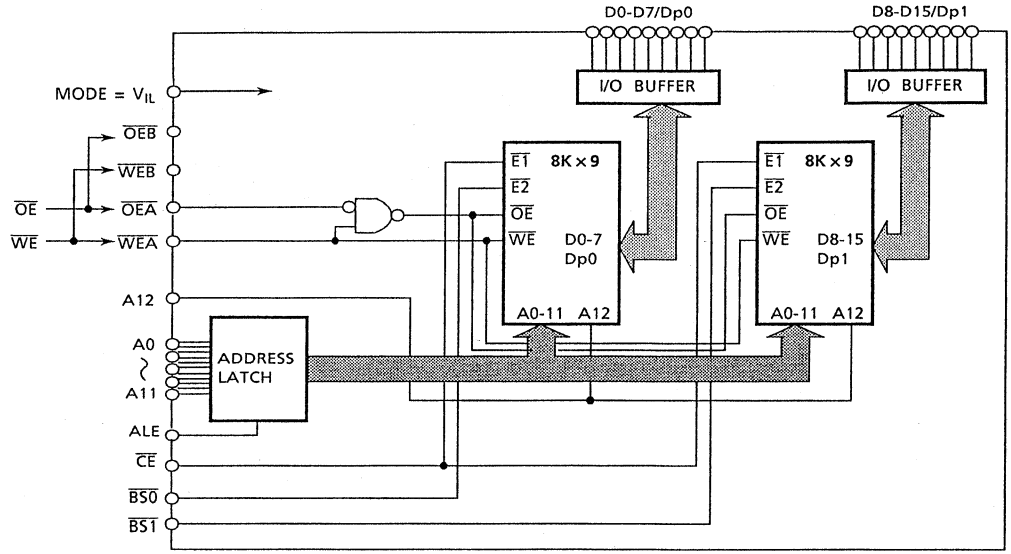
A0~A12	Address Inputs
D0~D15, DP0, DP1	Data Input / Output
ALE	Address Latch Input
$\overline{CE}$	Chip Enable Input
$\overline{BS0}$	Lower Byte Select Input
$\overline{BS1}$	Upper Byte Select input
$\overline{OEA}$	Output Enable Input (Way-A)
$\overline{OEB}$	Output Enable Input (Way-B)
$\overline{WEA}$	Write Enable Input (Way-A)
$\overline{WEB}$	Write Enable Input (Way-B)
MODE	Mode Select Input
VDD	Power (+5V)
GND	Ground

PIN CONNECTION (TOP VIEW)

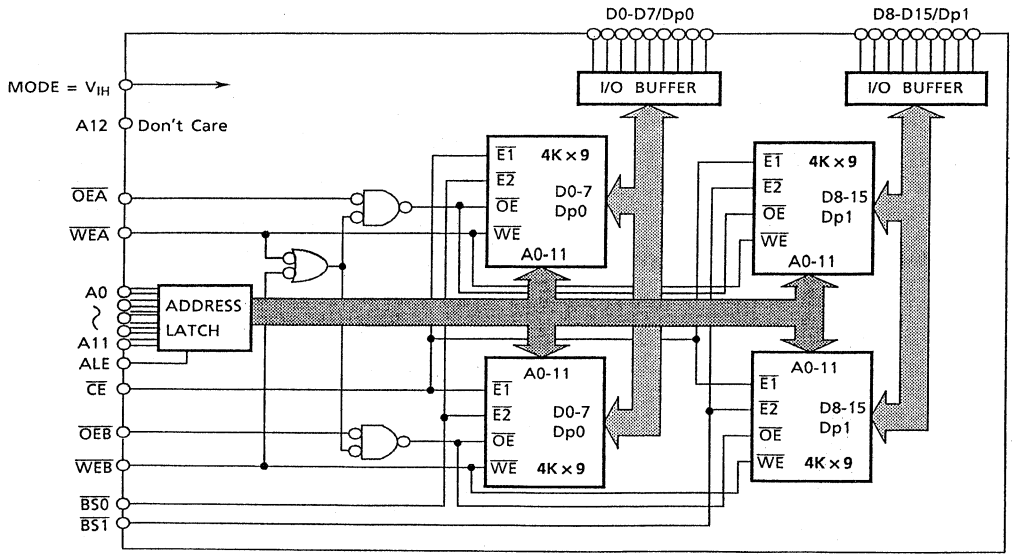


BLOCK DIAGRAM

1–WAY 8,192 words × 18 bits (MODE : V_{IL})



2–WAY 4,096 words × 18 bits (MODE : V_{IH})



TRUTH TABLE 1

CONTROL INPUT			FUNCTION			CONFIGURATION
MODE	ALE	$\overline{CE}$	CHIP	A0~A11	A12	
H	*1	H	Disable	*2	*2	4K × 18 × 2
H	H	L	Enable	Valid	*2	
H	L	L	Enable	Latched	*2	
L	*1	H	Disable	*2	*2	8K × 18
L	H	L	Enable	Valid	Valid	
L	L	L	Enable	Latched	Valid	

*1 : H or L *2 : Don't Care

TRUTH TABLE 2 (MODE = V_{IL} ··· 8K × 18)

INPUTS						OPERATION		
$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{BS0}$	$\overline{BS1}$	CHIP	D0-D7 Dp0	D8-D15 Dp1
*	*	*	*	H	H	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Open	Open
H	H	L	L	L	H	Read Cycle	Output	Open
				H	L		Open	Output
				L	L		Output	Output
L	L	*	*	L	H	Write Cycle	Input	Open
				H	L		Open	Input
				L	L		Input	Input
H	H	H	L	L	H	Undefine (9)	Undefine	Undefine
				H	L			
				L	L			
H	H	L	H	L	H	Undefine (9)	Undefine	Undefine
				H	L			
				L	L			
H	L	*	*	L	H	Undefine (8)	Undefine	Undefine
				H	L			
				L	L			
L	H	*	*	L	H	Undefine (8)	Undefine	Undefine
				H	L			
				L	L			

* : H or L

TRUTH TABLE 3 (MODE = V_{IH} ··· 4K x 18 x 2)

INPUTS						OPERATION			
$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{BS0}$	$\overline{BS1}$	way – A	way – B	D0~D7 Dp0	D8~D15 Dp1
*	*	*	*	H	H	Deselect	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Deselect	Open	Open
H	H	H	L	L	H	Deselect	Read Cycle	way – B Output	Open
				H	L			Open	way – B Output
				L	L			way – B Output	way – B Output
H	H	L	H	L	H	Read Cycle	Deselect	way – A Output	Open
				H	L			Open	way – A Output
				L	L			way – A Output	way – A Output
H	H	L	L	L	H	Deselect	Deselect	Open	Open
				H	L				
				L	L				
H	L	*	*	L	H	Deselect	Write Cycle	way – B Input	Open
				H	L			Open	way – B Input
				L	L			way – B Input	way – B Input
L	H	*	*	L	H	Write Cycle	Deselect	way – A Input	Open
				H	L			Open	way – A Input
				L	L			way – A Input	way – A Input
L	L	*	*	L	H	Write Cycle	Write Cycle	way – A/B Input	Open
				H	L			Open	way – A/B Input
				L	L			way – A/B Input	way – A/B Input

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD} + 0.5	V
P_D	Power Dissipation	1.3	W
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATION CONDITIONS (Ta = 0~70°C) (1)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	−0.5 *	−	0.8	V

* : −3V pulse width less than 10ns

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%) (1)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		−1	−	+1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	−	−	mA
I_{LO}	Output Leakage Current	Output Disable		−1	−	+1	μA
I_{DDO}	Operating Current	t_{RC}, t_{WC} = min. cycle Add., $\overline{WE}$, ALE = Clock (3.0V/0V) $\overline{OE}$ = 3.0V $\overline{CE}$, $\overline{BS}$ = 0V, MODE = 3.0V / 0V	−20	−	−	230	mA
			−25	−	−	220	
			−30	−	−	200	
I_{DDS}	Standby Current	$\overline{CE}$, $\overline{BS}$, $\overline{WE}$, $\overline{OE}$ = V_{IH}, ALE = V_{IL} Add., Data, MODE = V_{IH} or V_{IL}		−	−	40	mA

CAPACITANCE (Ta = 25°C, freq. = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Cin	Input Capacitance	V_{IN} = GND	−	−	5	pF
Cout	Output Capacitance	V_{OUT} = GND	−	−	7	pF

AC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%) (1)

READ CYCLE

SYMBOL	PARAMETER	-20		-25		-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	–	25	–	30	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	30	ns
t_{A12A}	A12 Access Time	–	15	–	17	–	20	ns
t_{LA}	ALE Access Time	–	20	–	25	–	30	ns
t_{CA}	$\overline{CE}$ Access Time	–	20	–	22	–	25	ns
t_{BA}	$\overline{BS}$ Access Time	–	20	–	22	–	25	ns
t_{OE}	$\overline{OE}$ Access Time	–	10	–	10	–	12	ns
t_{ASL}	Address Latch Set-Up Time	4	–	4	–	5	–	ns
t_{AHL}	Address Latch Hold Time	5	–	5	–	5	–	ns
t_{LP}	ALE Pulse Width	8	–	8	–	9	–	ns
t_{AOH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	ns
t_{LOH}	Output Data Hold Time from Address Latch	5	–	5	–	5	–	ns
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	5	–	5	–	5	–	ns
t_{BLZ}	$\overline{BS}$ to Output in Low-Z	5	–	5	–	5	–	ns
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns
t_{CHZ}	$\overline{CE}$ to Output in High-Z	–	10	–	10	–	12	ns
t_{BHZ}	$\overline{BS}$ to Output in High-Z	–	10	–	10	–	12	ns
t_{OHZ}	$\overline{OE}$ to Output in High-Z	–	8	–	8	–	10	ns
t_{OOI}	$\overline{OEA}/\overline{OEB}$ Inhibit Time	8	–	8	–	10	–	ns

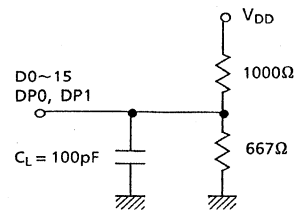
WRITE CYCLE

SYMBOL	PARAMETER	-20		-25		-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	–	25	–	30	–	ns
t_{WP}	$\overline{WE}$ Pulse Width	12	–	15	–	18	–	ns
t_{BW}	$\overline{BS}$ to End of Write	12	–	15	–	18	–	ns
t_{CW}	$\overline{CE}$ to End of Write	12	–	15	–	18	–	ns
t_{AW}	Write Address to End of Write	12	–	15	–	18	–	ns
t_{A12W}	Write Address A12 to End of Write	12	–	15	–	18	–	ns
t_{AS}	Write Address Set-Up Time	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{DS}	Data Set-Up Time	8	–	10	–	10	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	ns
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	–	5	–	5	–	ns
t_{WHZ}	$\overline{WE}$ to Output in High-Z	–	7	–	8	–	10	ns
t_{OEH}	$\overline{OE}$ Command Hold Time	5	–	5	–	5	–	ns
t_{WEH}	$\overline{WE}$ Command Hold Time	–	5	–	5	–	5	ns
t_{WI}	Write Command Inhibit Time	10	–	10	–	10	–	ns
t_{WA}	$\overline{WE}$ Access Time	–	20	–	25	–	30	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

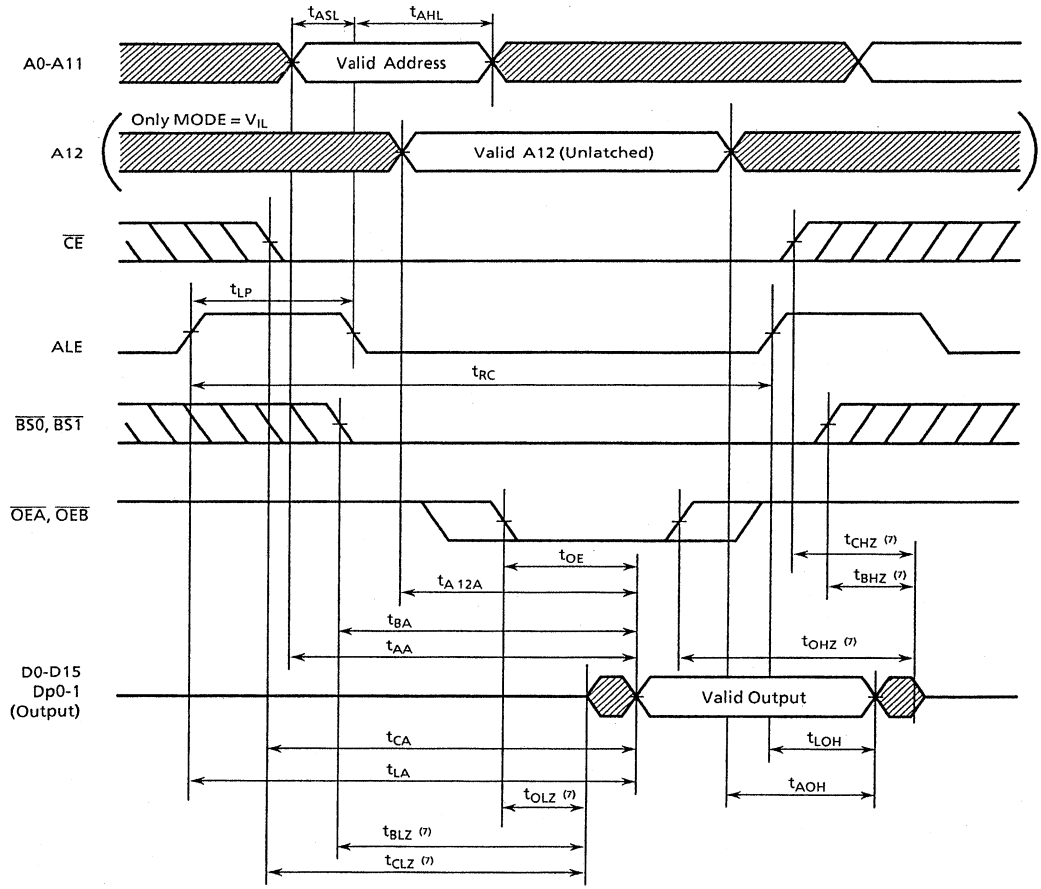
Fig. 1 OUTPUT LOAD



TIMING WAVEFORMS

READ CYCLE TIMING 1

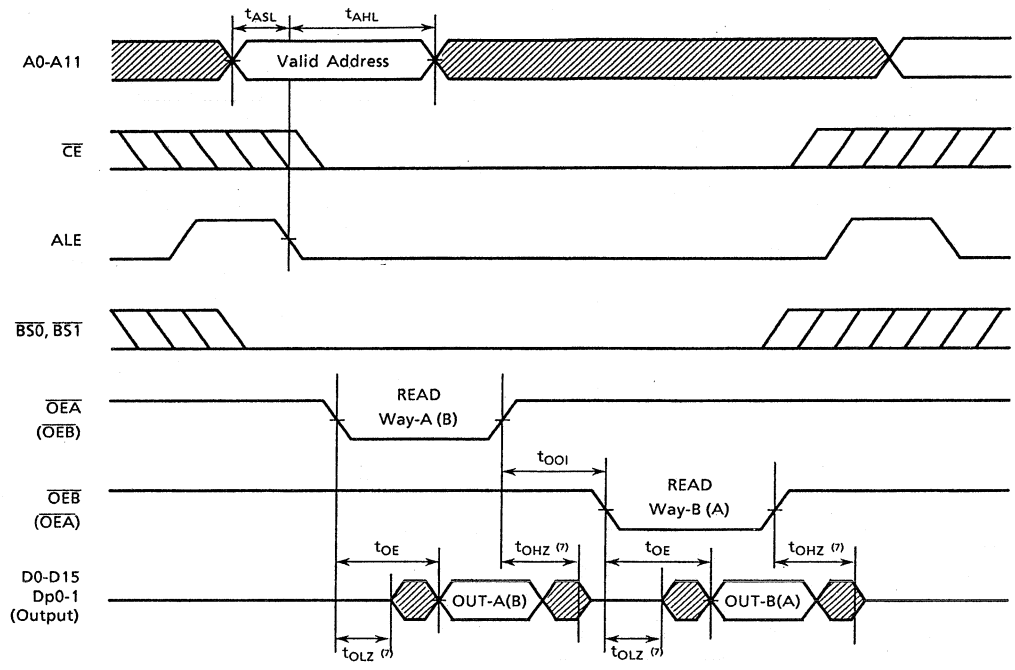
MODE = V_{IH} ··· 4K × 18 × 2 (A12 = Don't Care)
MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)



NOTE : $\overline{WEA}$, $\overline{WEB}$ = V_{IH}

··· Don't Care

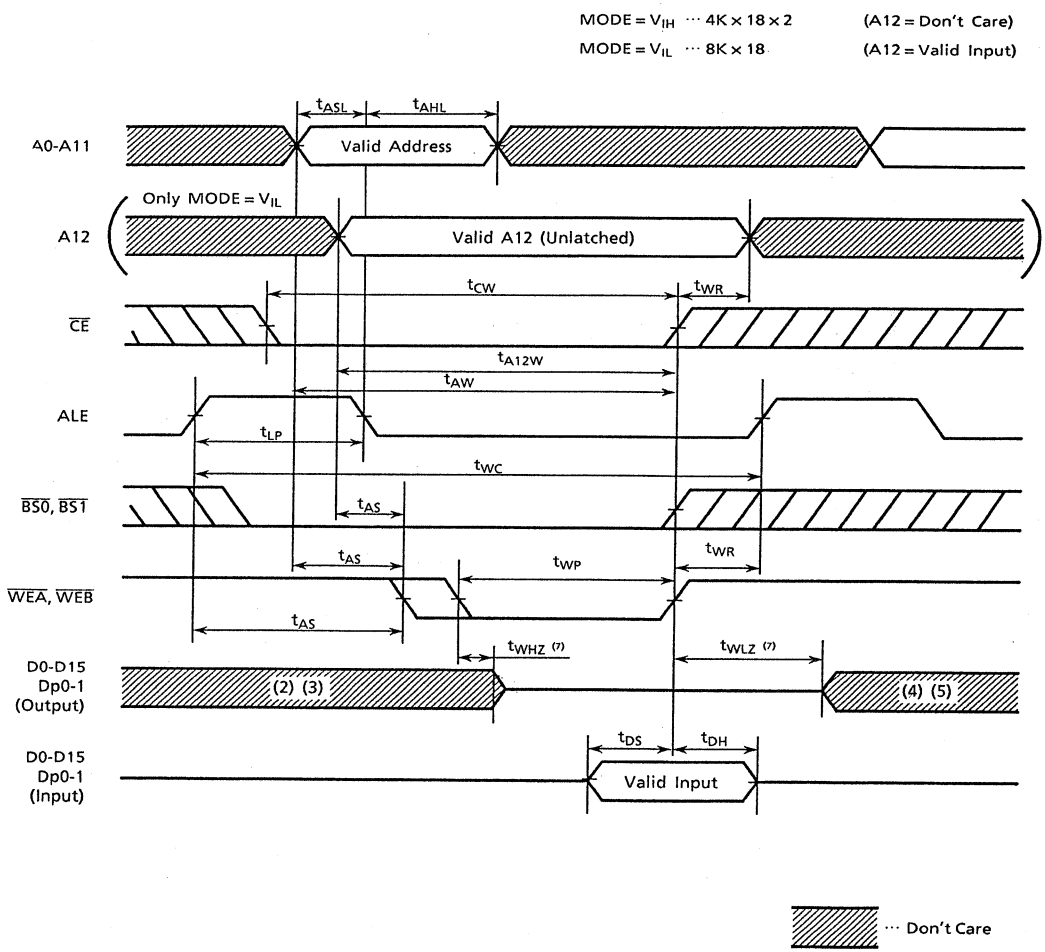
READ CYCLE TIMING 2 (t_{OOI} TIMING . MODE = V_{IH})



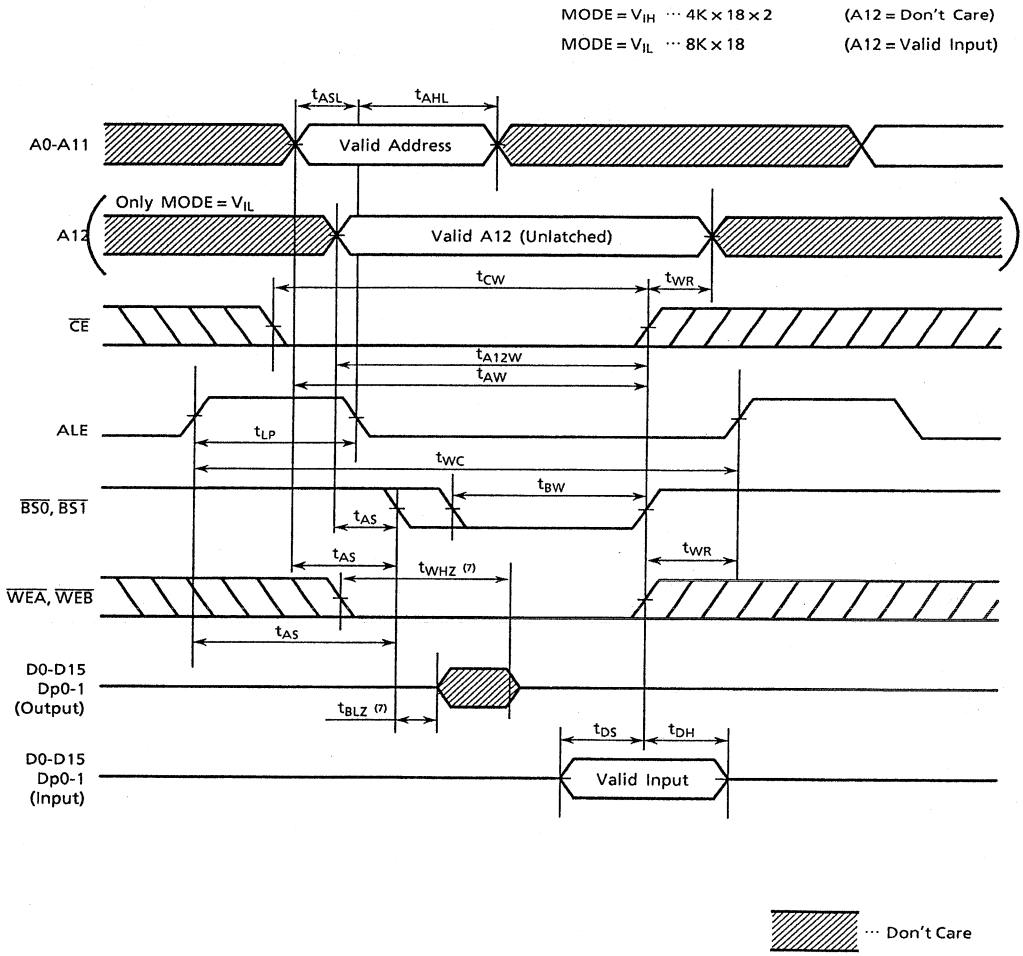
NOTE : $\overline{WEA}$, $\overline{WEB}$ = V_{IH}

··· Don't Care

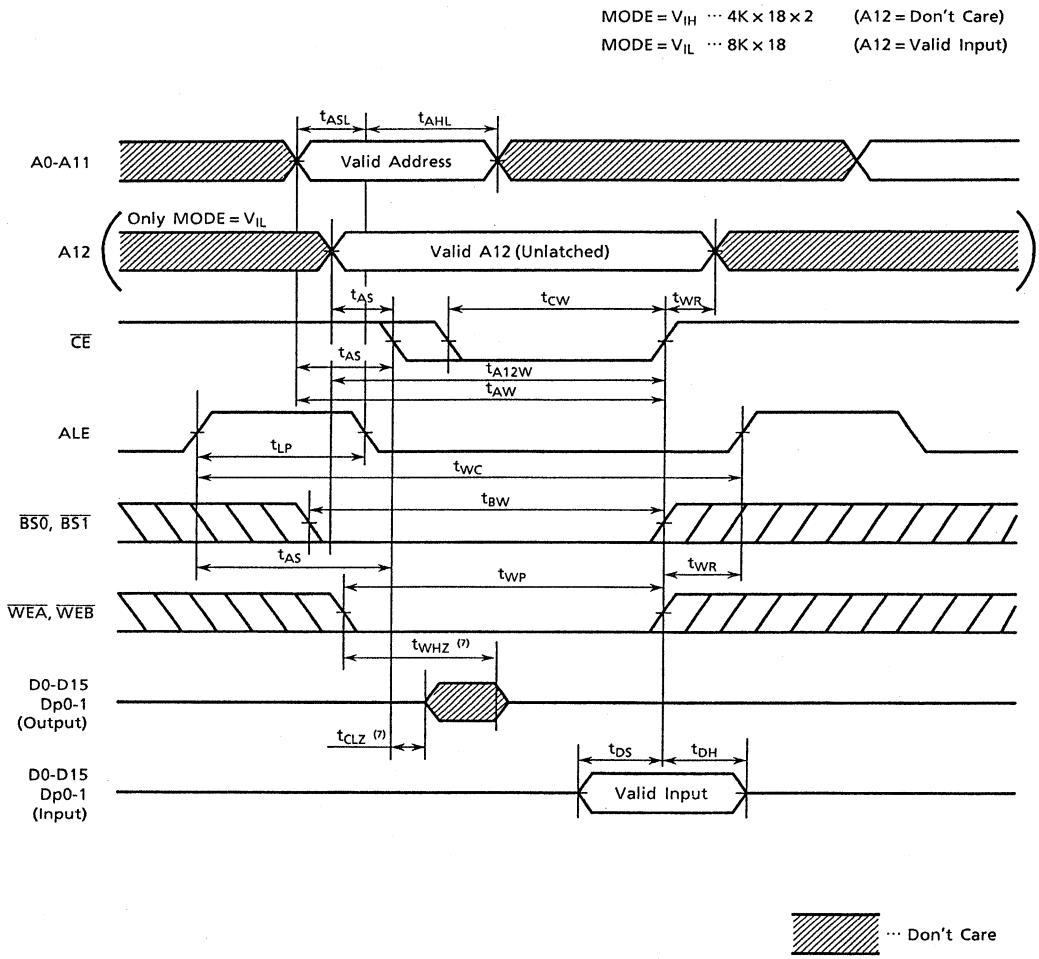
WRITE CYCLE TIMING 1 ($\overline{WE}$ Control) (6)



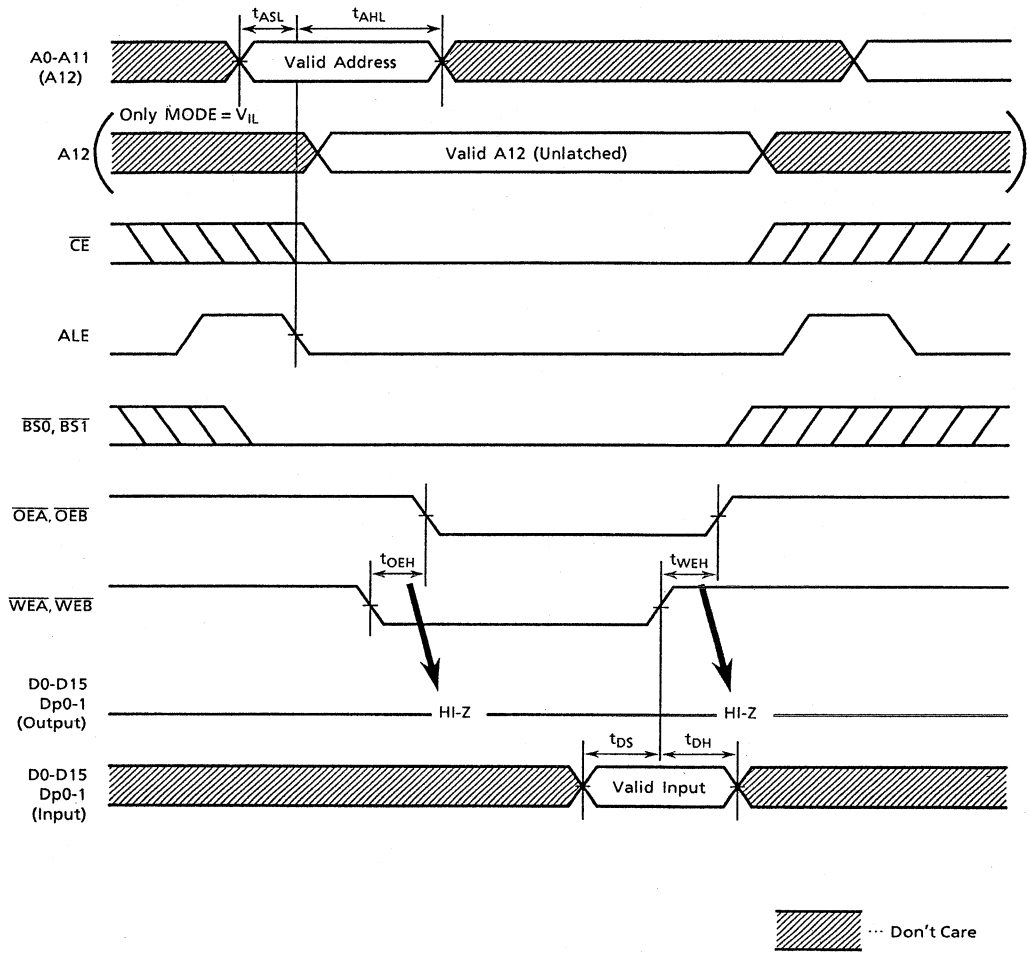
WRITE CYCLE TIMING 2 ($\overline{BS}$ Control) (6)



WRITE CYCLE TIMING 3 ($\overline{CE}$ Control) (6)

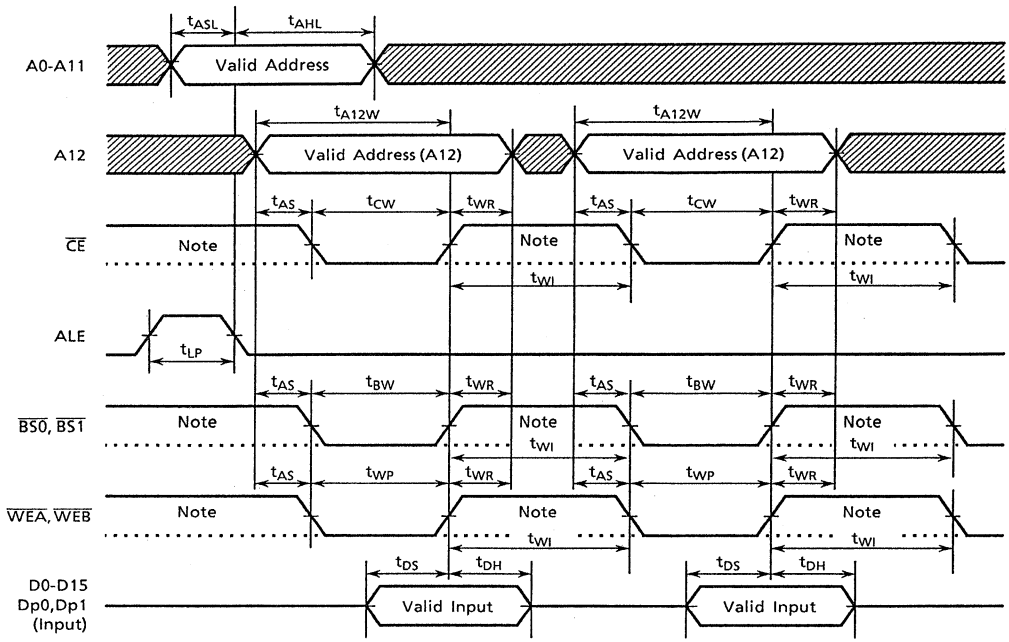


WRITE CYCLE TIMING 4 (t_{OEH} and t_{WEH}) (6)



WRITE CYCLE TIMING 5 (A12 Control) (6)

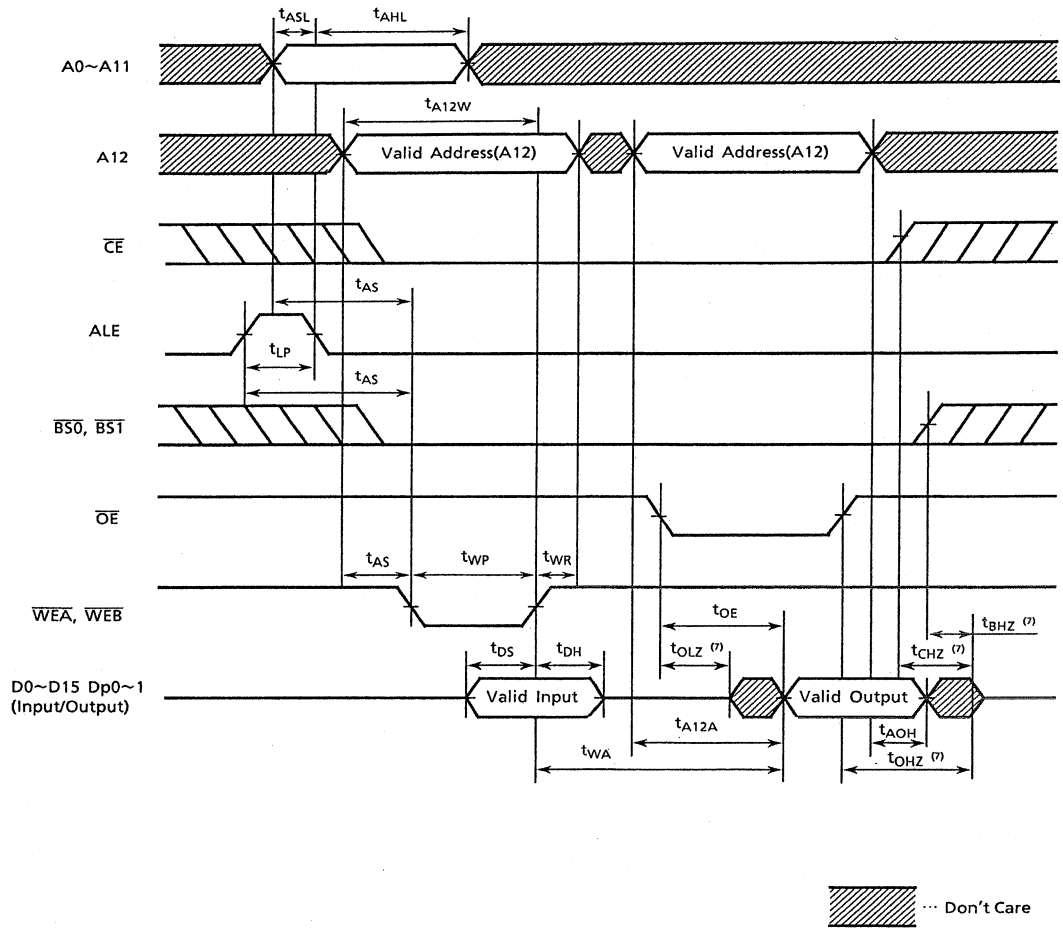
Only MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)



Note ; t_{WI} ··· Write Command Inhibit Time
($\overline{CE}$ = H or $\overline{BS0}$ = $\overline{BS1}$ = H or $\overline{WEA}$ = $\overline{WEB}$ = H)

··· Don't Care

READ AFTER WRITE CYCLE TIMING



NOTE : 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{BS0}$ or $\overline{BS1}$ Low transition occur coincident with or after $\overline{WE}$ transition, Lower Byte Outputs (D0~D7, Dp0) or Upper Byte Outputs (D8~D15, Dp1) remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

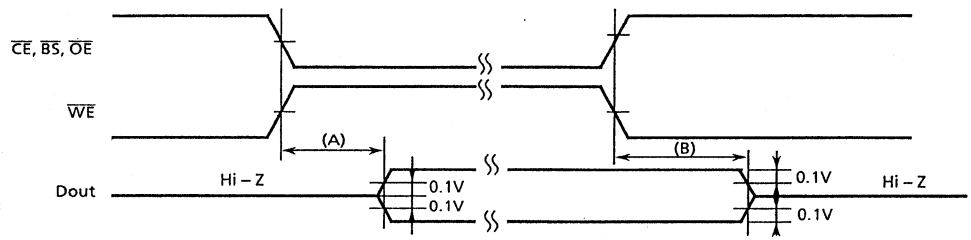
5. Assuming that $\overline{BS0}$ or $\overline{BS1}$ High transition occurs coincident with or prior to $\overline{WE}$ transition, Lower Byte Outputs (D0~D7, Dp0) or Upper Byte Outputs (D8~D15, Dp1) remain in a high impedance state.

6. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

7. These parameters are specified as follows and measured by using load shown in Fig. 1.

   (A) t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{WLZ} ··· Output Enable Time

   (B) t_{CHZ}, t_{BHZ}, t_{OHZ}, t_{WHZ} ··· Output Disable Time



8. The Write Data and Write Address are indeterminate when the input level of $\overline{WEA}$ and $\overline{WEB}$ is diferent on Direct Mapping Mode (MODE = V_{IL}).

9. The Read Data are indeterminate when the input level of $\overline{OEA}$ and $\overline{OEB}$ is diferent on Direct Mapping Mode (MODE = V_{IL}).

TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

We hope this information will be very useful for you.

Nov. 1991

TOSHIBA CORPORATION
Semiconductor Group

Unit in mm

QFJ52-P-S750