

# TC55188T-20,-25,-35

2 - WAY 4,096 WORDS × 18 BITS / 8,192 WORDS × 18 BITS  
 CMOS STATIC CACHE DATA RAM

## DESCRIPTION

The TC55188T is a 147,456bits high-speed static RAM which can be user-configured either as 2-way 4,096 words by 18 bits or as 8,192 words by 18 bits. It is provided with a byte control, on-chip address latches and chip-enable latch. The TC55188T is fabricated using Toshiba's CMOS technology and advanced circuit techniques which provide the high speed feature, and is operated from a single 5-volt supply. This device features address access time as fast as 20ns, output-enable access as fast as 10ns and simple interfacing capability with bipolar TTL circuits. The TC55188T can directly interface with the INTEL 82385 cache controller, without requiring additional peripheral circuit such as latches, transceivers and gates. Therefore; Significant reductions in the number of parts, board assembly area and power dissipation can be achieved by using the TC55188T cache data RAM. The MODE input of the TC55188T allows the user to configure the memory internally either as a 2-way 4,096 words by 18 bits organization which is suitable for 2-way set associative cache designs or as a 8,192 words by 18 bits organization suitable for direct map cache designs. The TC55188T can also be operated as a conventional asynchronous static RAM, which can be accessed from change of address, by holding the ALE input in the high state. The TC55188T is packaged in a 52-pin standard PLCC for high-density board level assembly.

## FEATURES

- Fast Access Time (max.)

ITEM	TC55188T		
	- 20	- 25	- 30
t <sub>RC</sub> Cycle Time	20ns	25ns	30ns
t <sub>AA</sub> Address Access Time	20ns	25ns	30ns
t <sub>OE</sub> OE Access Time	10ns	10ns	12ns

- Power dissipation
 

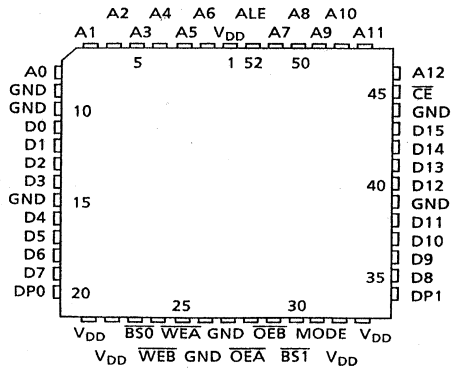
Operating	TC55188T-20	230mA (max.)
	TC55188T-25	220mA (max.)
	TC55188T-30	200mA (max.)
Standby		40mA (max.)

- Configurable for 2-way or direct RAM arrays  
 2-way 4,096words×18bits (MODE=V<sub>IH</sub>)  
 8,192words×18bits (MODE=V<sub>IL</sub>)
- Contains address latches, CE latch and byte control, BS0 and BS1
- Interfaces directly with the Intel 82385 Cache Controller
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- Two Output buffer controls : OEA, OEB
- Two Write enable controls : WEA, WEB
- TC55188T : QFJ-P-S750

## PIN NAMES

A0~A12	Address Inputs
D0~D15, DP0, DP1	Data Input/Output
ALE	Address/CE Latch Input
CE	Chip Enable Input
BS0	Lower Byte Select Input
BS1	Upper Byte Select input
OEA	Output Enable Input (Way - A)
OEB	Output Enable Input (Way - B)
WEA	Write Enable Input (Way - A)
WEB	Write Enable Input (Way - B)
MODE	Mode Select Input
VDD	Power (+ 5V)
GND	Ground

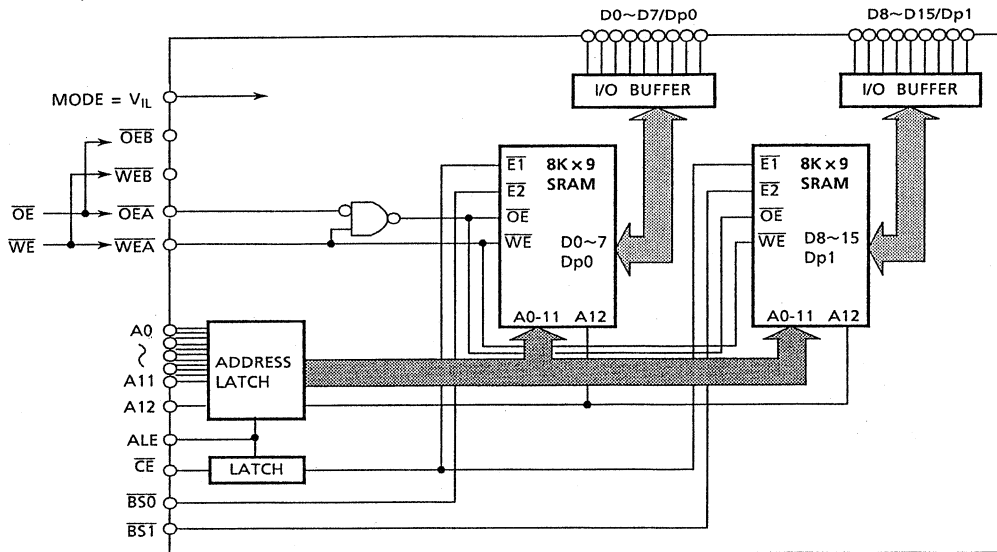
## PIN CONNECTION (TOP VIEW)



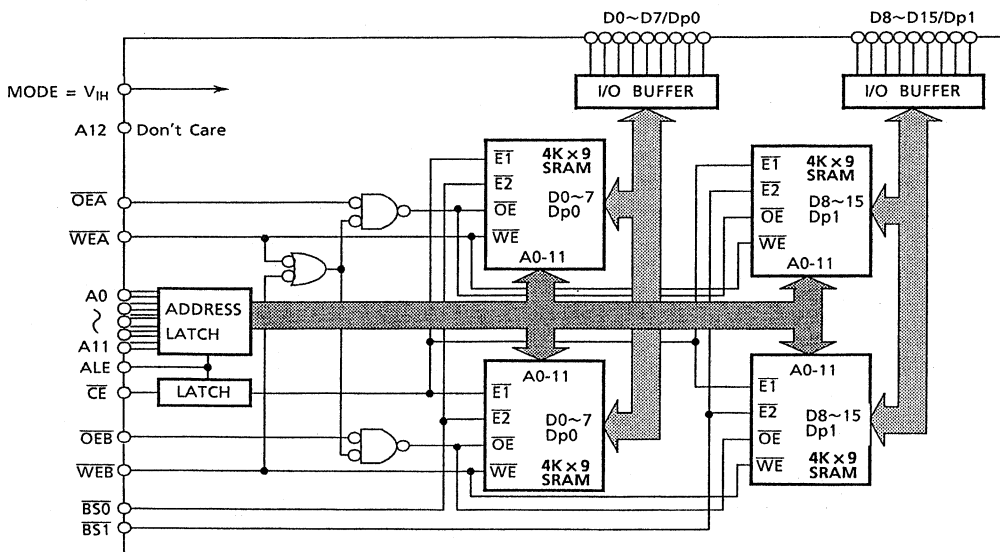
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## BLOCK DIAGRAM

1-WAY 8,192 words  $\times$  18 bits (MODE :  $V_{IL}$ )



2-WAY 4,096 words  $\times$  18 bits (MODE :  $V_{IH}$ )



TRUTH TABLE 1

CONTROL INPUT			FUNCTION			CONFIGURATION
MODE	ALE	CE	CHIP	A0~A11	A12	
H	H	H	Disable	*1	*1	4K × 18 × 2
H	H	L	Enable	Valid	*1	
H	L	H*2	Disable	Latched	Latched	
H	L	L*2	Enable	Latched	Latched	
L	H	H	Disable	*1	*1	8K × 18
L	H	L	Enable	Valid	Valid	
L	L	H*2	Disable	Latched	Latched	
L	L	L*2	Enable	Latched	Latched	

\* 1 : Don't Care

\* 2 : Latched level as ALE from H to L

TRUTH TABLE 2 (MODE = V<sub>IL</sub> ... 8K × 18)

INPUTS						OPERATION		
WEA	WEB	OE A	OE B	BS0	BS1	CHIP	D0~D7 Dp0	D8~D15 Dp1
*	*	*	*	H	H	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Open	Open
H	H	L	L	L	H	Read Cycle	Output	Open
				H	L		Open	Output
				L	L		Output	Output
L	L	*	*	L	H	Write Cycle	Input	Open
				H	L		Open	Input
				L	L		Input	Input
H	H	H	L	L	H	Undefined (9)	Undefined	Undefined
				H	L			
				L	L			
H	H	L	H	L	H	Undefined (9)	Undefined	Undefined
				H	L			
				L	L			
H	L	*	*	L	H	Undefined (8)	Undefined	Undefined
				H	L			
				L	L			
L	H	*	*	L	H	Undefined (8)	Undefined	Undefined
				H	L			
				L	L			

\* : H or L

TRUTH TABLE 3 (MODE = V<sub>IH</sub> ... 4K x 18 x 2)

INPUTS						OPERATION			
WEA	WEB	OE <sub>A</sub>	OE <sub>B</sub>	B <sub>S0</sub>	B <sub>S1</sub>	way - A	way - B	D0~D7 Dp0	D8~D15 Dp1
*	*	*	*	H	H	Deselect	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Deselect	Open	Open
H	H	H	L	L	H	Deselect	Read Cycle	way - B Output	Open
				H	L			Open	way - B Output
				L	L			way - B Output	way - B Output
H	H	L	H	L	H	Read Cycle	Deselect	way - A Output	Open
				H	L			Open	way - A Output
				L	L			way - A Output	way - A Output
H	H	L	L	L	H	Deselect	Deselect	Open	Open
				H	L				
				L	L				
H	L	*	*	L	H	Deselect	Write Cycle	way - B Input	Open
				H	L			Open	way - B Input
				L	L			way - B Input	way - B Input
L	H	*	*	L	H	Write Cycle	Deselect	way - A Input	Open
				H	L			Open	way - A Input
				L	L			way - A Input	way - A Input
L	L	*	*	L	H	Write Cycle	Write Cycle	way - A/B Input	Open
				H	L			Open	way - A/B Input
				L	L			way - A/B Input	way - A/B Input

\* : Don't Care

**MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.5~7.0	V
V <sub>IN</sub>	Input Voltage	-2.0~7.0	V
V <sub>OUT</sub>	Output Voltage	-0.5~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.3	W
T <sub>solder</sub>	Soldering Temperature · Time	260 · 10	°C · sec
T <sub>strg</sub>	Storage Temperature	-65~150	°C
T <sub>opr</sub>	Operating Temperature	-10~85	°C

**DC RECOMMENDED OPERATION CONDITIONS (Ta = 0~70°C) (1)**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5*	-	0.8	V

\* : -3V pulse width less than 10ns.

**DC CHARACTERISTICS (Ta = 0~70°C, V<sub>DD</sub> = 5V ± 10%) (1)**

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0~V <sub>DD</sub>	-1	-	+1	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-4	-	-	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	8	-	-	mA	
I <sub>LO</sub>	Output Leakage Current	Output Disable	-1	-	+1	μA	
I <sub>DDO</sub>	Operating Current	t <sub>RC</sub> , t <sub>WC</sub> = min. cycle Add., $\overline{WE}$ , ALE = Clock (3V/0V) $\overline{OE}$ = 3.0V $\overline{CE}$ , $\overline{BS}$ = 0V, MODE = 3.0V/0V	-20	-	-	230	mA
			-25	-	-	220	
			-30	-	-	200	
I <sub>DDs</sub>	Standby Current	$\overline{CE}$ , $\overline{BS}$ , $\overline{WE}$ , $\overline{OE}$ = V <sub>IH</sub> , ALE = V <sub>IL</sub> Add., Data, MODE = V <sub>IH</sub> or V <sub>IL</sub>	-	-	40	mA	

**CAPACITANCE (Ta = 25°C, freq. = 1MHz)**

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C <sub>in</sub>	Input Capacitance	V <sub>IN</sub> = GND	-	-	5	pF
C <sub>out</sub>	Output Capacitance	V <sub>OUT</sub> = GND	-	-	7	pF

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## AC CHARACTERISTICS (Ta = 0~70°C, V<sub>DD</sub> = 5V ± 10%) (1)

### READ CYCLE

SYMBOL	PARAMETER	- 20		- 25		- 30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	20	-	25	-	30	-	ns
t <sub>AA</sub>	Address Access Time	-	20	-	25	-	30	ns
t <sub>LA</sub>	ALE Access Time	-	20	-	25	-	30	ns
t <sub>CA</sub>	$\overline{CE}$ Access Time	-	20	-	22	-	25	ns
t <sub>BA</sub>	$\overline{BS}$ Access Time	-	20	-	22	-	25	ns
t <sub>OE</sub>	$\overline{OE}$ Access Time	-	10	-	10	-	12	ns
t <sub>ASL</sub>	Address Latch Set-Up Time	4	-	4	-	5	-	ns
t <sub>AHL</sub>	Address Latch Hold Time	5	-	5	-	5	-	ns
t <sub>LP</sub>	ALE Pulse Width	8	-	8	-	9	-	ns
t <sub>AOH</sub>	Output Data Hold Time from Address Change	5	-	5	-	5	-	ns
t <sub>LOH</sub>	Output Data Hold Time from Address Latch	5	-	5	-	5	-	ns
t <sub>LLZ</sub>	ALE to Output in Low-Z	5	-	5	-	5	-	ns
t <sub>CLZ</sub>	$\overline{CE}$ to Output in Low-Z	5	-	5	-	5	-	ns
t <sub>BLZ</sub>	$\overline{BS}$ to Output in Low-Z	5	-	5	-	5	-	ns
t <sub>OLZ</sub>	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns
t <sub>LHZ</sub>	ALE to Output in High-Z	-	12	-	12	-	15	ns
t <sub>CHZ</sub>	$\overline{CE}$ to Output in High-Z	-	10	-	10	-	12	ns
t <sub>BHZ</sub>	$\overline{BS}$ to Output in High-Z	-	10	-	10	-	12	ns
t <sub>OHZ</sub>	$\overline{OE}$ to Output in High-Z	-	8	-	8	-	10	ns
t <sub>OI</sub>	$\overline{OE}/\overline{OEB}$ Inhibit Time	8	-	8	-	10	-	ns

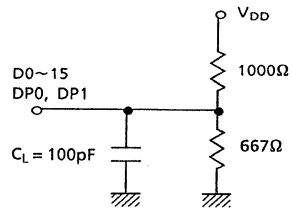
WRITE CYCLE

SYMBOL	PARAMETER	- 20		- 25		- 30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	20	–	25	–	30	–	ns
t <sub>WP</sub>	$\overline{WE}$ Pulse Width	12	–	15	–	18	–	ns
t <sub>BW</sub>	$\overline{BS}$ to End of Write	12	–	15	–	18	–	ns
t <sub>CV</sub>	$\overline{CE}$ to End of Write	12	–	15	–	18	–	ns
t <sub>AW</sub>	Write Address to End of Write	12	–	15	–	18	–	ns
t <sub>AS</sub>	Write Address Set-Up Time	0	–	0	–	0	–	ns
t <sub>WR</sub>	Write Recovery Time	0	–	0	–	0	–	ns
t <sub>DS</sub>	Data Set-Up Time	8	–	10	–	10	–	ns
t <sub>DH</sub>	Data Hold Time	0	–	0	–	0	–	ns
t <sub>WLZ</sub>	$\overline{WE}$ to Output in Low-Z	5	–	5	–	5	–	ns
t <sub>WHZ</sub>	$\overline{WE}$ to Output in High-Z	–	7	–	8	–	10	ns
t <sub>OEH</sub>	$\overline{OE}$ Command Hold Time	5	–	5	–	5	–	ns
t <sub>WEH</sub>	$\overline{WE}$ Command Hold Time	–	5	–	5	–	5	ns
t <sub>WI</sub>	Write Command Inhibit Time	10	–	10	–	10	–	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

Fig. 1 OUTPUT LOAD

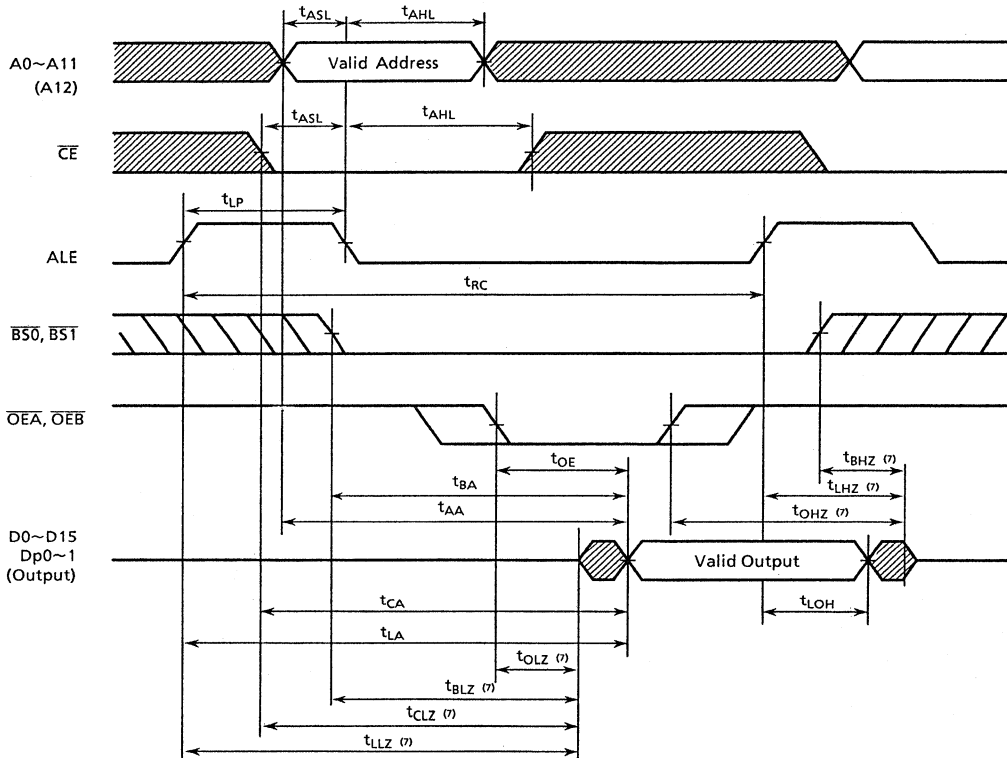


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## TIMING WAVEFORMS

### READ CYCLE TIMING 1 (ALE = Clock)

MODE =  $V_{IH}$  ... 4K x 18 x 2 (A12 = Don't Care)  
 MODE =  $V_{IL}$  ... 8K x 18 (A12 = Valid Input)



NOTE :  $\overline{WEA}, \overline{WEB} = V_{IH}$

 ... Don't Care



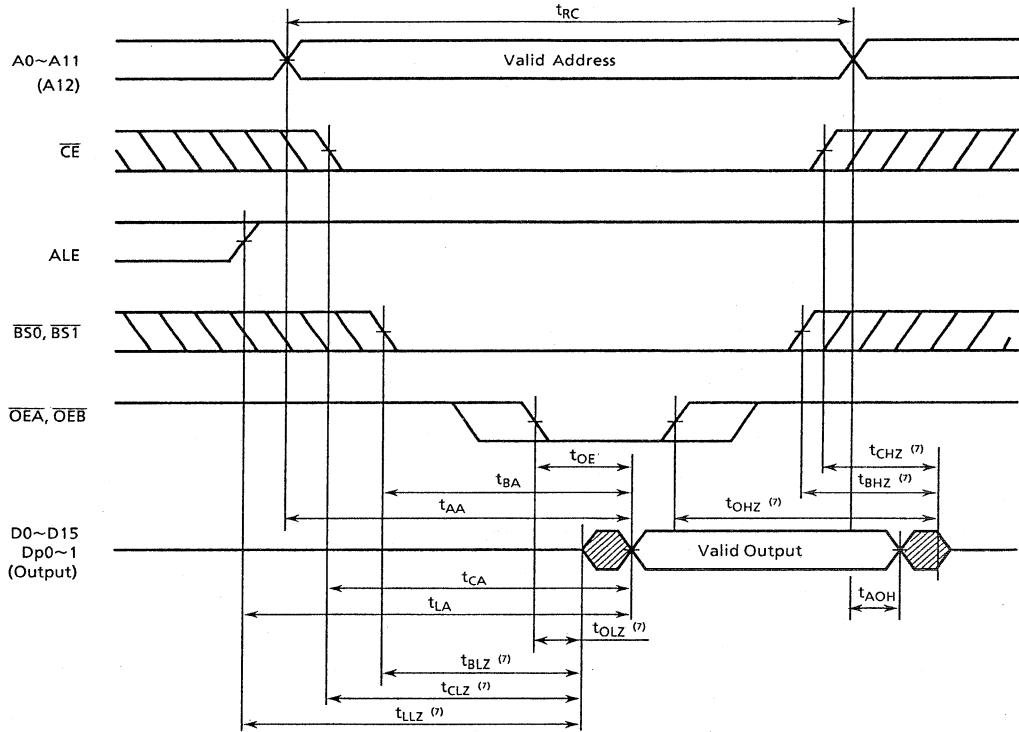
READ CYCLE TIMING 2 (ALE = V<sub>IH</sub>)

MODE = V<sub>IH</sub> ... 4K × 18 × 2

(A12 = Don't Care)

MODE = V<sub>IL</sub> ... 8K × 18

(A12 = Valid Input)

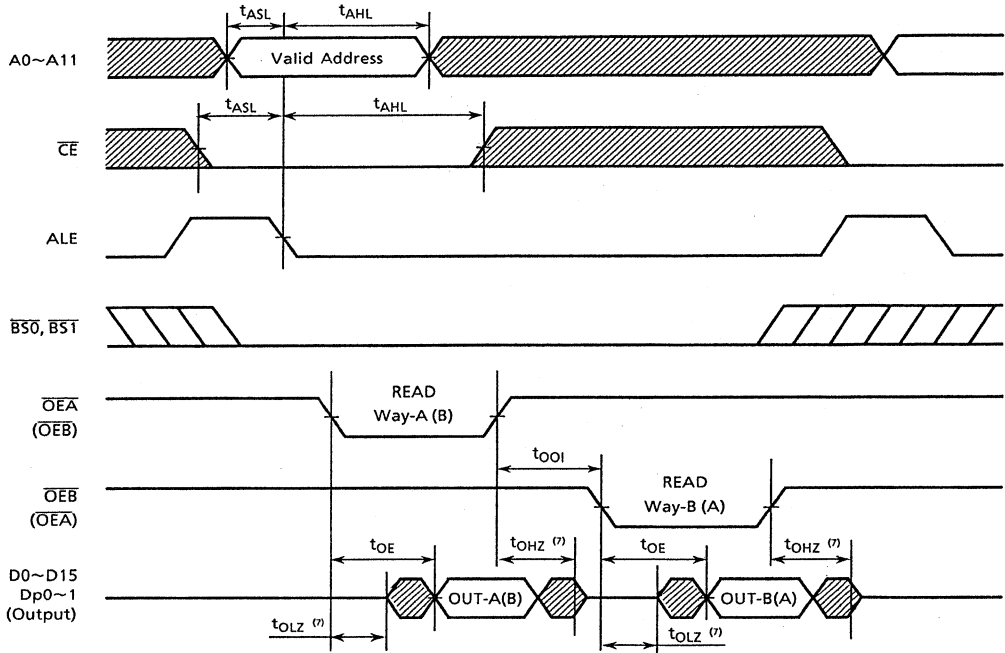


NOTE :  $\overline{WEA}, \overline{WEB} = V_{IH}$

 ... Don't Care

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READ CYCLE TIMING 3 ( $t_{OOI}$  TIMING, MODE =  $V_{IH}$ )

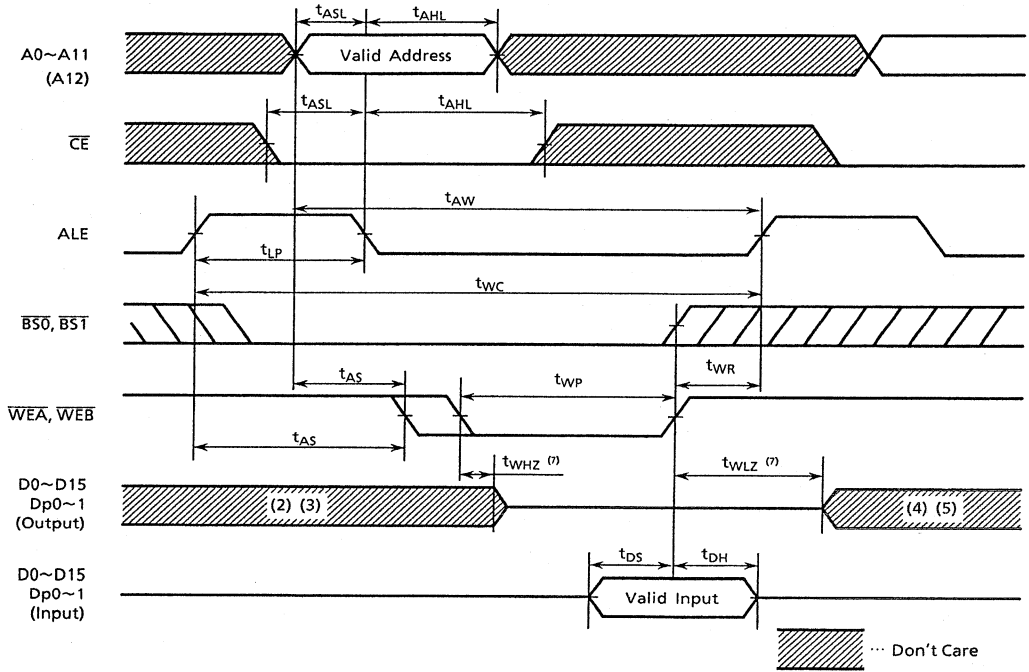


NOTE :  $\overline{WEA}, \overline{WEB} = V_{IH}$

... Don't Care

WRITE CYCLE TIMING 1 ( $\overline{WE}$  Control) (6)

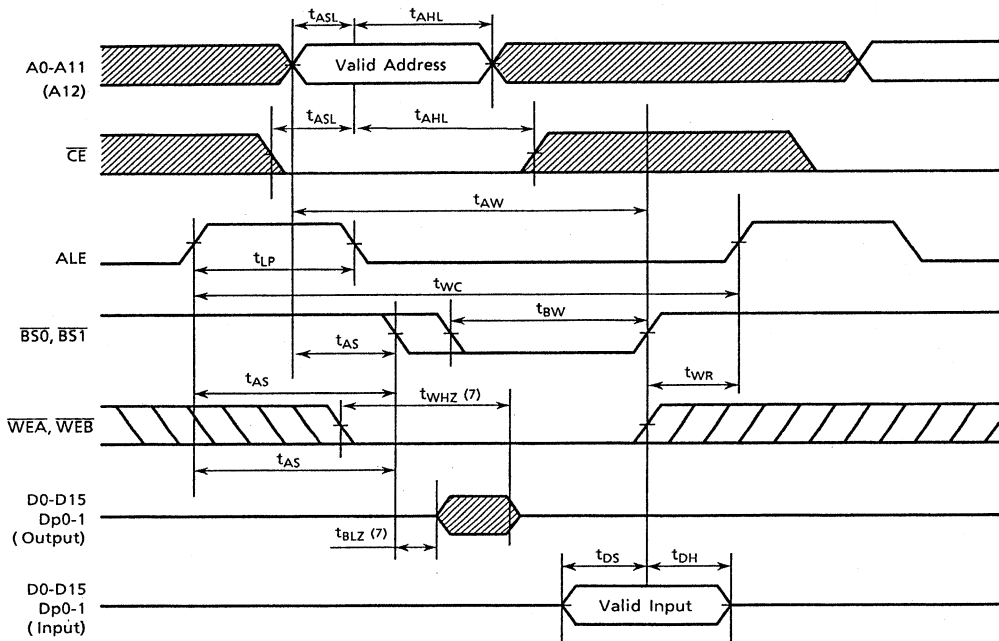
MODE =  $V_{IH}$  ... 4K x 18 x 2 (A12 = Don't Care)  
 MODE =  $V_{IL}$  ... 8K x 18 (A12 = Valid Input)




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## WRITE CYCLE TIMING 2 ( $\overline{BS}$ Control) (6)

MODE =  $V_{IH}$  ... 4K x 18 x 2 (A12 = Don't Care)  
 MODE =  $V_{IL}$  ... 8K x 18 (A12 = Valid Input)

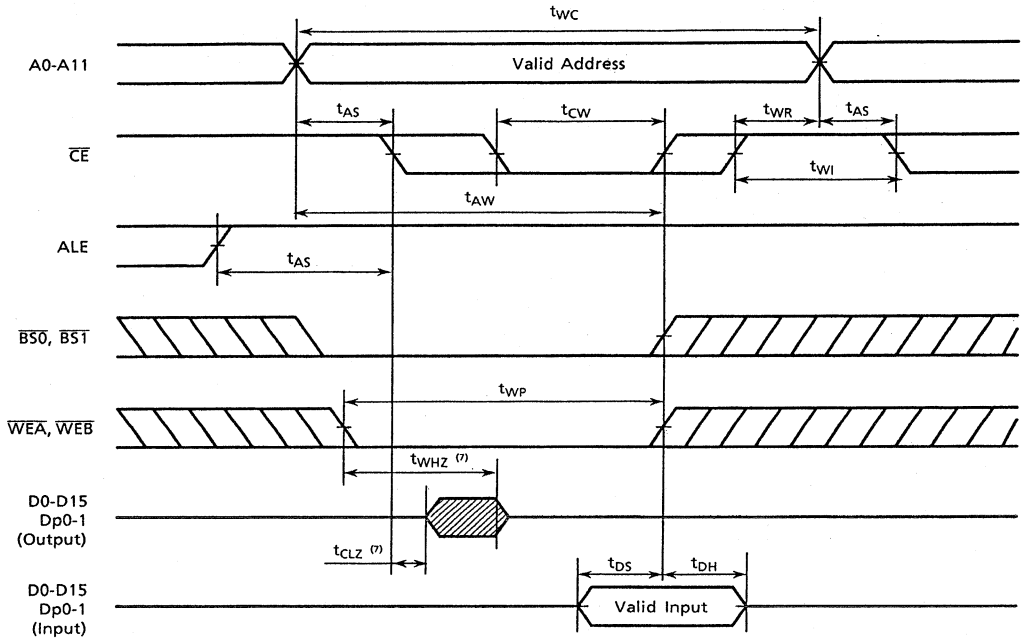


 ... Don't Care

WRITE CYCLE TIMING 3 ( $\overline{CE}$  Control) (6)

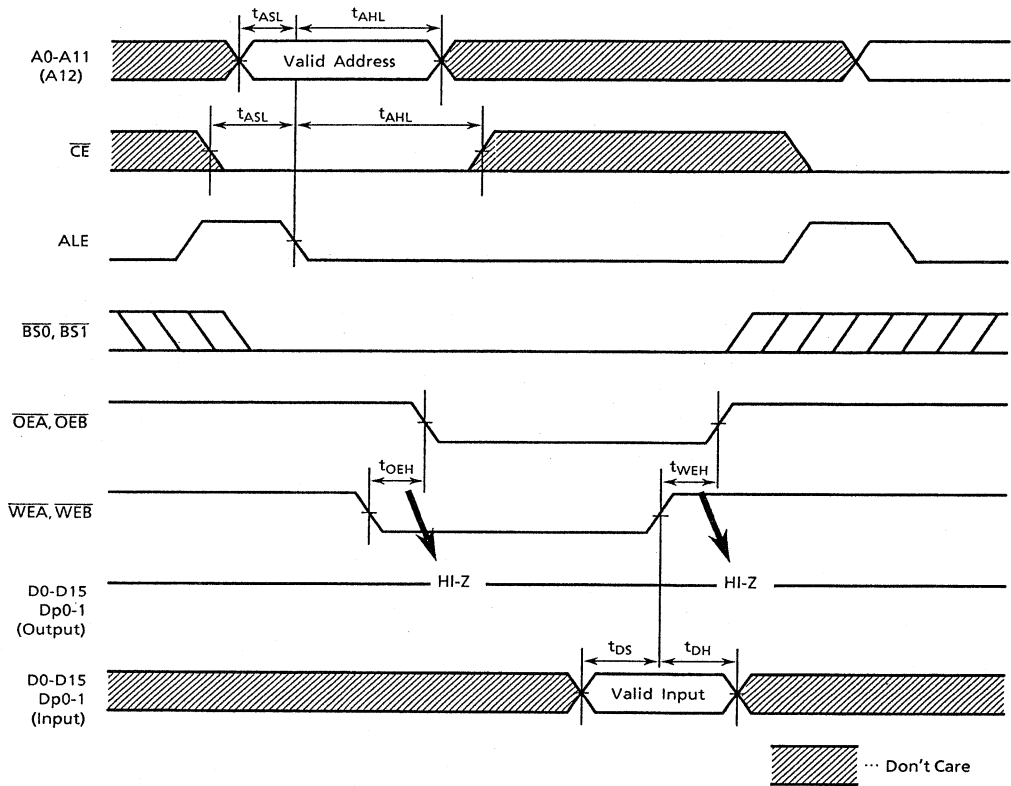
MODE =  $V_{IH}$  ... 4K x 18 x 2 (A12 = Don't Care)

MODE =  $V_{IL}$  ... 8K x 18 (A12 = Valid Input)



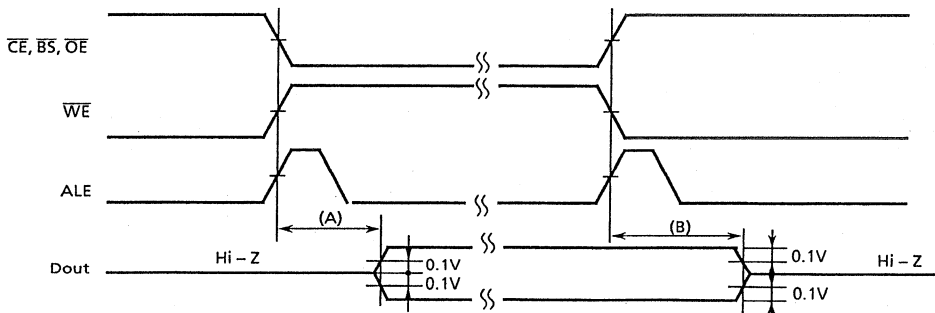
 ... Don't Care

WRITE CYCLE TIMING 4 ( $t_{OE\bar{H}}$  and  $t_{WE\bar{H}}$ ) (6)



- NOTE : 1. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Assuming that  $\overline{CE}$  Low transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{BS0}$  or  $\overline{BS1}$  Low transition occur coincident with or after  $\overline{WE}$  transition, Lower Byte Outputs (D0~D7, Dp0) or Upper Byte Outputs (D8~D15, Dp1) remain in a high impedance state.
4. Assuming that  $\overline{CE}$  High transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
5. Assuming that  $\overline{BS0}$  or  $\overline{BS1}$  High transition occurs coincident with or prior to  $\overline{WE}$  transition, Lower Byte Outputs (D0~D7, Dp0) or Upper Byte Outputs (D8~D15, Dp1) remain in a high impedance state.
6. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in a high impedance state during this period.
7. These parameters are specified as follows and measured by using load shown in Fig. 1.

- (A)  $t_{LLZ}$ ,  $t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{WLZ}$  ... Output Enable Time
- (B)  $t_{LHZ}$ ,  $t_{CHZ}$ ,  $t_{BHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  ... Output Disable Time



\* The relation between signals depends on the preceding Timing Charts.

8. The Write Data and Write Address are indeterminate when the input level of  $\overline{WEA}$  and  $\overline{WEB}$  is different on Direct Mapping Mode (MODE =  $V_{IL}$ ).
9. The Read Data are indeterminate when the input level of  $\overline{OEA}$  and  $\overline{OEB}$  is different on Direct Mapping Mode (MODE =  $V_{IL}$ ).

**TOSHIBA**

DATA BOOK

**MOS MEMORY**  
(VRAM, SRAM)

**1991**



# INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

We hope this information will be very useful for you.

Nov. 1991

TOSHIBA CORPORATION  
Semiconductor Group

Unit in mm

QFJ52-P-S750

