TC55257BPL/BFL/BSPL-85,-10
TC55257BFTL/BTRL-85,-10

TENTATIVE DATA

32,768 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC55257BPL is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5 V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5 mA / MHz (Typ.) and minimum cycle time of 85 ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 100 μA. The TC55257BPL has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257BPL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257BPL is offered in a standard dual-in-line 28 pin plastic package (0.6 / 0.3 inch width), small-out-line plastic package and thin-small-out-line plastic package (forward type, reverse type).

FEATURES

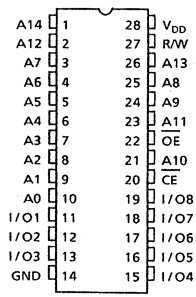
- Low Power Dissipation
  27.5 mW / MHz (Typ.) Operating
- Standby Current : 100 μA (MAX.)
- 5 V Single Power Supply
- Power Down Feature : $\overline{CE}$
- Data retention Supply Voltage : 2.0~5.5 V
- Directly TTL Compatible
  : All Inputs and Outputs
- Access Time

	TC55257BPL/BFL/ BSPL/BFTL/BTRL - 85	TC55257BPL/BFL/ BSPL/BFTL/BTRL - 10
Access Time (max.)	85 ns	100 ns
Chip Enable Access Time (max.)	85 ns	100 ns
Output Enable Time (max.)	45 ns	50 ns

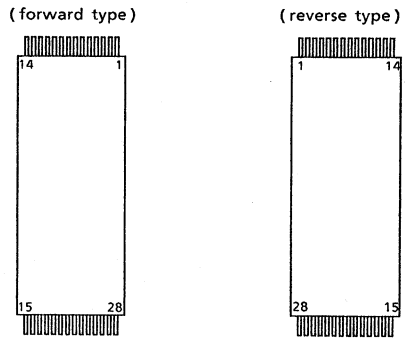
- Package
  TC55257BPL : DIP28-P-600
  TC55257BFL : SOP28-P-450
  TC55257BSPL : DIP28-P-300B
  TC55257BFTL : TSOP28-P
  TC55257BTRL : TSOP28-P-A

PIN CONNECTION (TOP VIEW)

o 28 PIN DIP & SOP



o 28 PIN TSOP

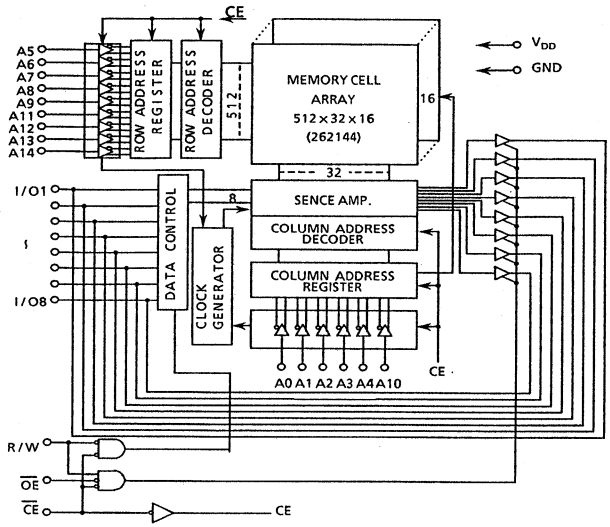


PIN NAME

A0~A14	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1~I/O8	Data Input / Output
V_{DD}	Power (+ 5 V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A_{11}	A_9	A_8	A_{13}	R/W	V_{DD}	A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_3
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* : H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.8/0.6**	W
Tsolder	Soldering Temperature	260・10	°C・sec
Tstrg	Storage Temperature	−55~150	°C
Topr	Operating Temperature	0~70	°C

* : −3.0 V at pulse width 50 ns
** : 0.6 inch 1.0 W, 0.3 inch 0.8 W, 0.45 inch 0.6 W

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	– 0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* : – 3.0 V at pulse width 50 ns

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70$ °C, $V_{DD} = 5$ V ± 10 %)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		–	–	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4$ V		– 1.0	–	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4$ V		4.0	–	–	mA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V_{IL} or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$		–	–	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ R/W = V_{IH} Other Input = V_{IH} / V_{IL} I_{OUT} = 0 mA	t_{cycle} = 1 μs	–	10	–	mA
			t_{cycle} = Min. cycle	–	–	70	
I_{DDO2}		$\overline{CE}$ = 0.2 V R/W = V_{DD} – 0.2 V Other Input = V_{DD} – 0.2 V / 0.2 V I_{OUT} = 0 mA	t_{cycle} = 1 μs	–	5	–	mA
			t_{cycle} = Min. cycle	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		–	–	3	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2$, V_{DD} = 2.0V~5.5V, Ta = 0~70 °C		–	2	100	μA

CAPACITANCE ($Ta = 25$ °C, $f = 1$ MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note : This parameter periodically sampled is not 100 % tested.

A.C. CHARACTERISTICS (Ta = 0~70 °C, V_{DD} = 5 V ± 10 %)

Read Cycle

SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL-85		TC55257BPL/BFL/BSPL/BFTL/BTRL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO}	$\overline{CE}$ Access Time	–	85	–	100	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	30	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	30	–	40	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

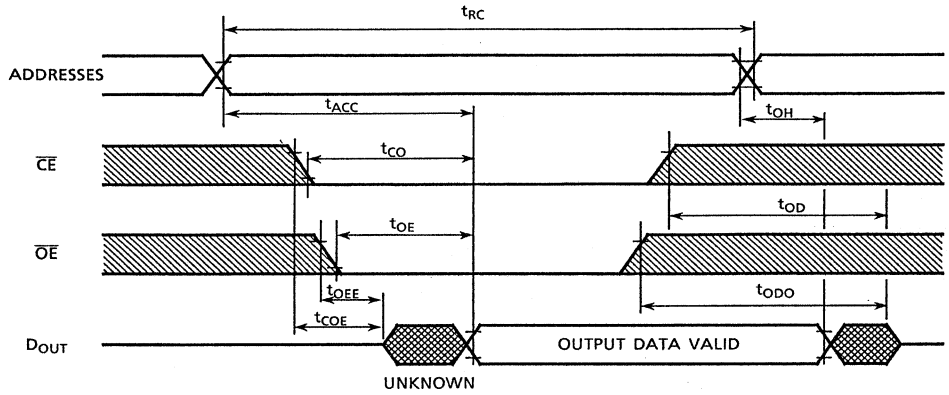
SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL-85		TC55257BPL/BFL/BSPL/BFTL/BTRL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	
t_{CW}	Chip Selection to End of Write	65	–	90	–	
t_{AS}	Address Set up Time	0	–	0	–	
t_{WR}	Write Recovery Time	5	–	5	–	
t_{ODW}	R/W to Output in High-Z	–	30	–	50	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	
t_{DS}	Data Set up Time	40	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

A.C. Test Conditions

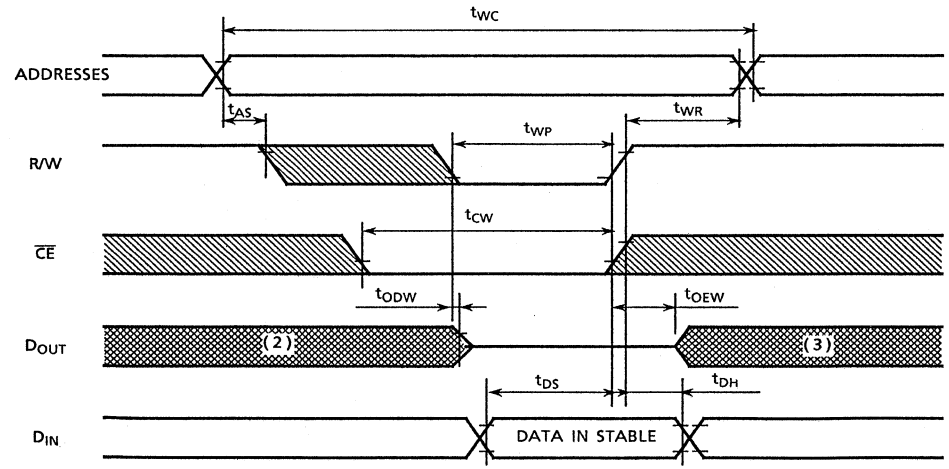
Output Load	:	100 pF + 1 TTL Gate
Input Pulse Level	:	0.6 V, 2.4 V
Timing Measurement	:	0.8 V, 2.2 V
Reference Level	:	0.8 V, 2.2 V
t_r, t_f	:	5 ns

TIMING WAVEFORMS

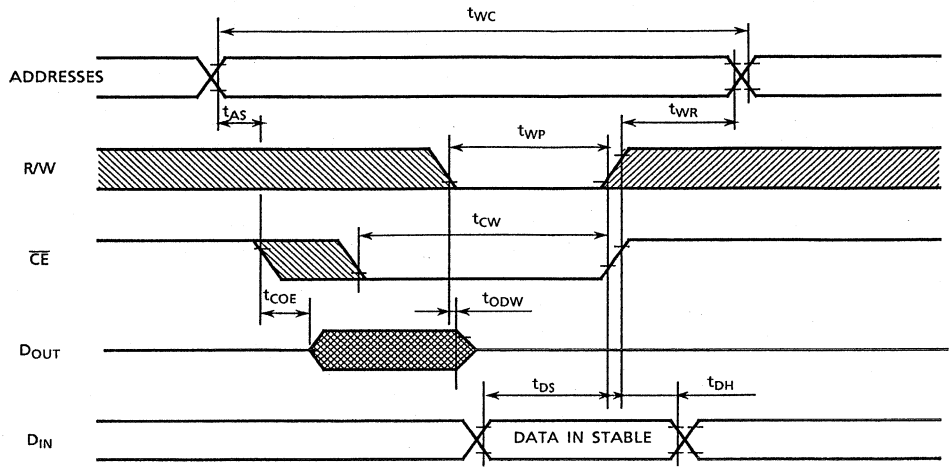
Read Cycle (1)



Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 (4) ($\overline{CE}$ Controlled Write)



Note : (1) R/W is High for read cycle.

(2) Assuming that $\overline{CE}$ low transition occurs coincident with or after R / W Low transition, Outputs remain a high impedance state.

(3) Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R / W High transition, Outputs remain a high impedance state.

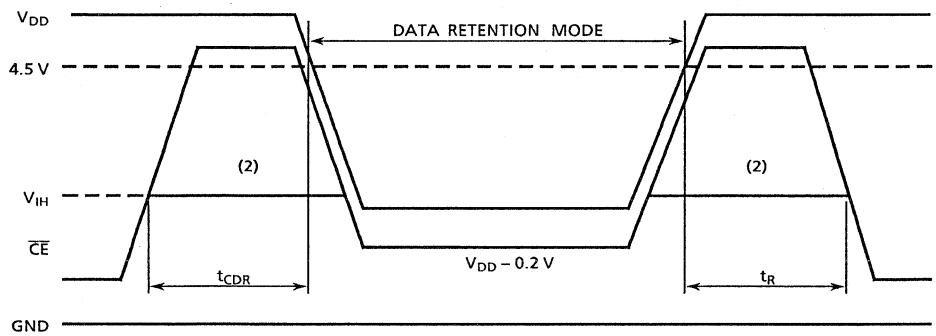
(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = 0~70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Supply Current	V_{DH} = 3.0 V	–	–	50	μA
		V_{DH} = 5.5 V	–	–	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	–	–	μS
t_R	Recovery Time		t_{RC} (1)	–	–	

Note (1) : Read Cycle Time.

$\overline{CE}$ Controlled Data Retention Mode



Note (2) : If the V_{IH} of $\overline{CE}$ is 2.2 V in opertion, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5 V to 2.4 V

TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

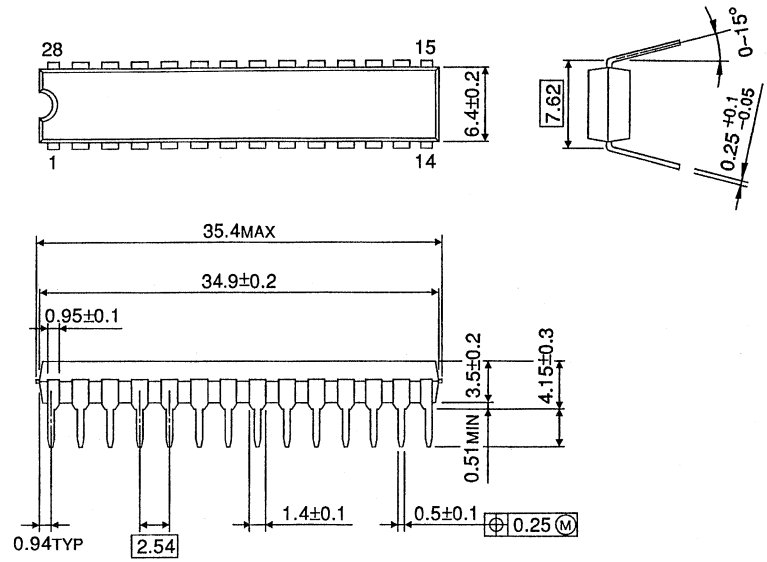
We hope this information will be very useful for you.

Nov. 1991

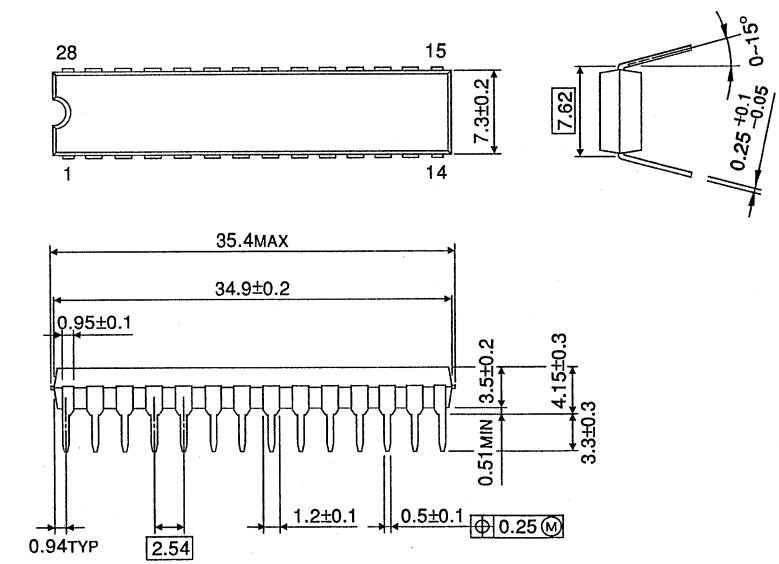
TOSHIBA CORPORATION
Semiconductor Group

Unit in mm

DIP28-P-300A

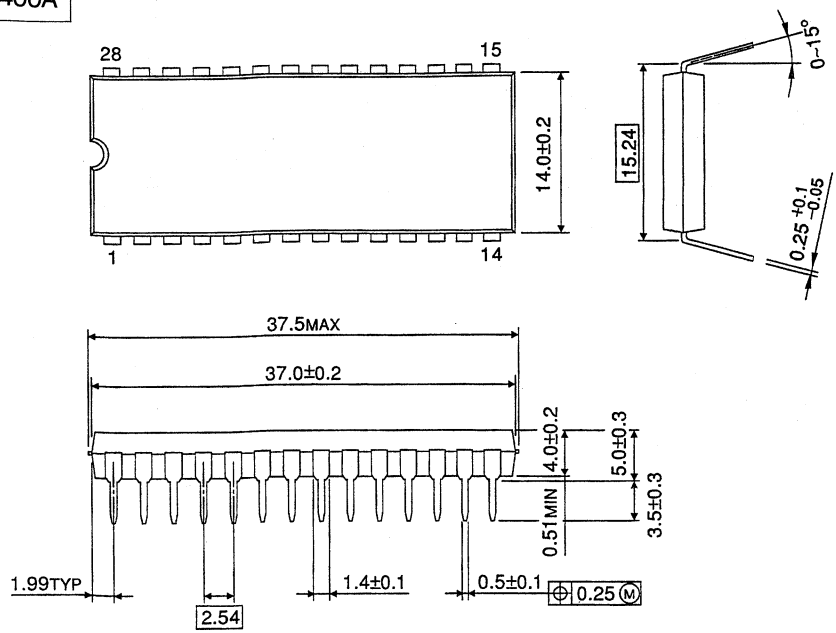


DIP28-P-300B

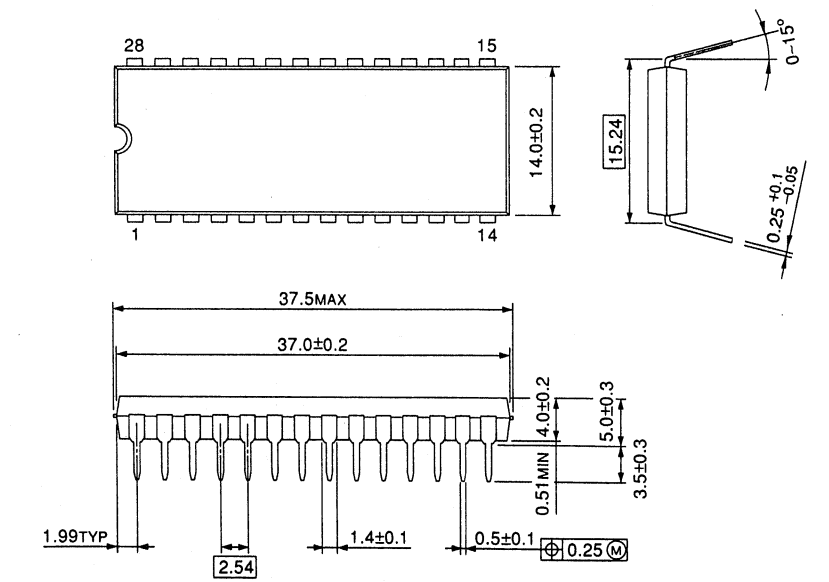


Unit in mm

DIP28-P-400A

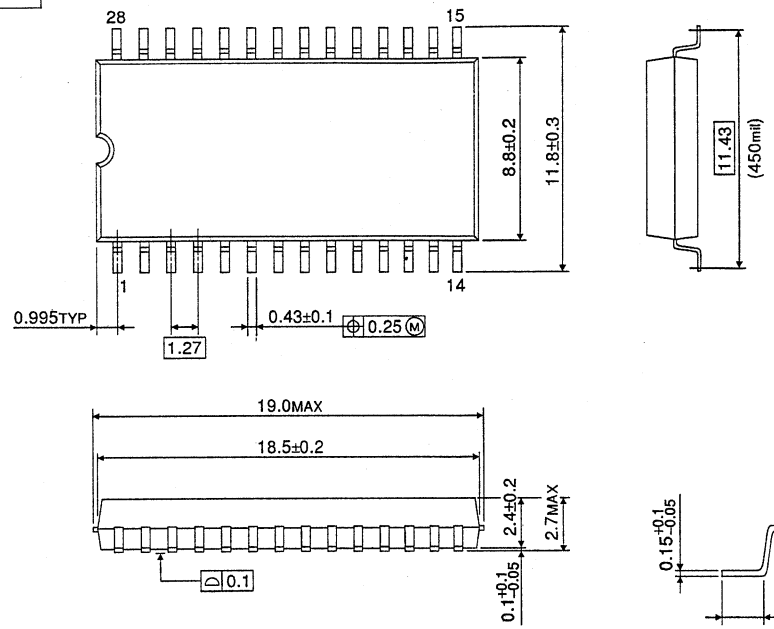


DIP28-P-600

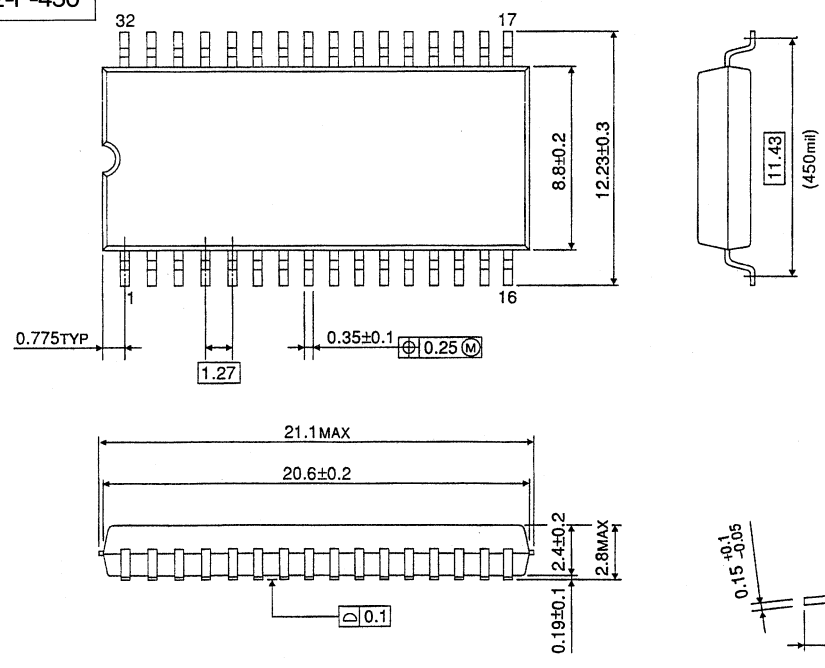


Unit in mm

SOP28-P-450



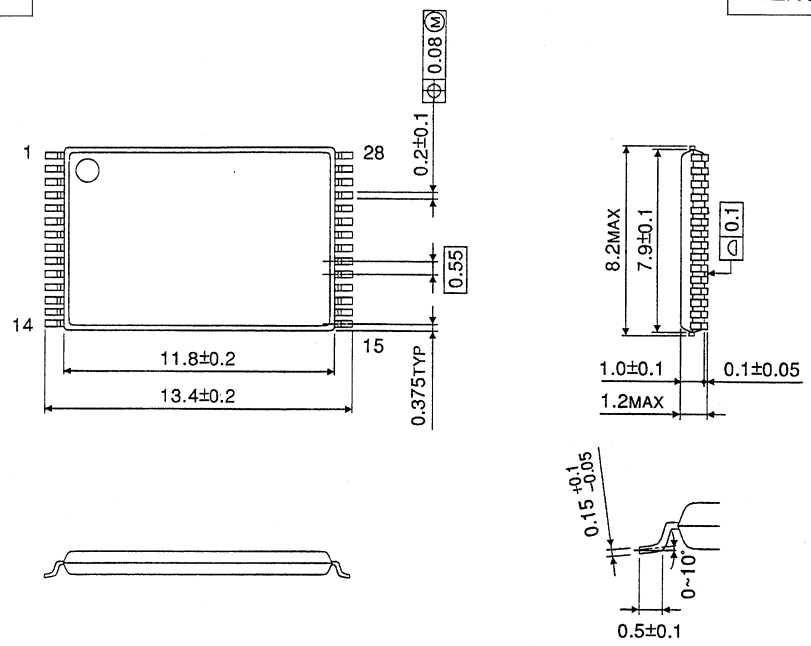
SOP32-P-450



Unit in mm

TSOP28-P

TENTATIVE



TSOP28-P-A

TENTATIVE