

# TC55257BPL/BFL/BSPL-85L,-10L TC55257BFTL/BTRL-85L,-10L

TENTATIVE DATA

32,768 WORDS × 8 BIT STATIC RAM

## DESCRIPTION

The TC55257BPL is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5 V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5 mA/MHz (Typ.) and minimum cycle time of 85 ns.

When  $\overline{CE}$  is a logical high, the device is placed in low power standby mode in which standby current is  $2\mu\text{A}$  at room temperature. The TC55257BPL has two control inputs. Chip enable ( $\overline{CE}$ ) allows for device selection and data retention control, and an output enable input ( $\overline{OE}$ ) provides fast memory access. Thus the TC55257BPL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257BPL is offered in a standard dual-in-line 28 pin plastic package (0.6/0.3 inch width), small-out-line plastic package and thin-small-out-line plastic package (forward type, reverse type).

## FEATURES

- Low Power Dissipation  
27.5 mW/MHz (Typ.) Operating
- Standby Current :  $2\mu\text{A}$  (MAX.) at  $T_a = 25^\circ\text{C}$
- 5 V Single Power Supply
- Power Down Feature :  $\overline{CE}$
- Data retention Supply Voltage : 2.0~5.5 V
- Directly TTL Compatible  
: All Inputs and Outputs

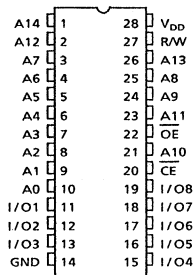
## • Access Time

	TC55257BPL/BFL/ BSPL/BFTL/BTRL - 85L	TC55257BPL/BFL/ BSPL/BFTL/BTRL - 10L
Access Time (max.)	85 ns	100 ns
Chip Enable Access Time (max.)	85 ns	100 ns
Output Enable Time (max.)	45 ns	50 ns

- Package TC55257BPL : DIP28-P-600  
TC55257BFL : SOP28-P-450  
TC55257BSPL : DIP28-P-300B  
TC55257BFTL : TSOP28-P  
TC55257BTRL : TSOP28-P-A

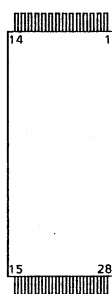
## PIN CONNECTION (TOP VIEW)

○ 28 PIN DIP & SOP

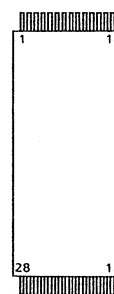


○ 28 PIN TSOP

(forward type)



(reverse type)



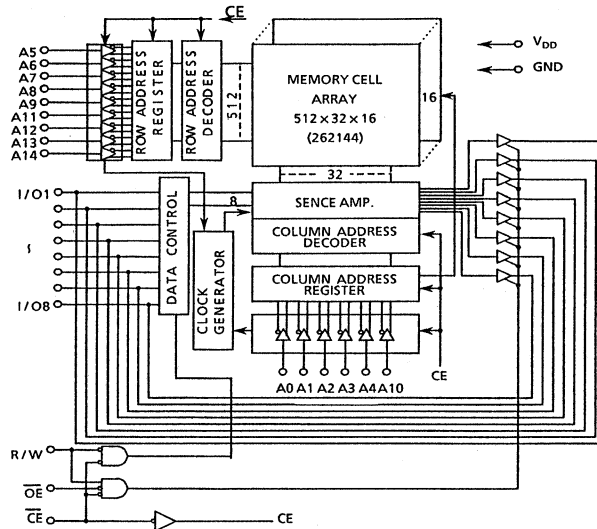
## PIN NAME

A0~A14	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1~I/O8	Data Input / Output
$V_{DD}$	Power (+ 5 V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A <sub>11</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>13</sub>	R/W	$V_{DD}$	A <sub>14</sub>	A <sub>12</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A <sub>10</sub>

# TC55257BPL/BFL/BSPL-85L,-10L TC55257BFTL/BTRL-85L,-10L

## BLOCK DIAGRAM



## OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	D <sub>OUT</sub>	I <sub>DD0</sub>
Write	L	*	L	D <sub>IN</sub>	I <sub>DD0</sub>
Output Deselect	L	H	H	High-Z	I <sub>DD0</sub>
Standby	H	*	*	High-Z	I <sub>DD5</sub>

\* : H or L

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	-0.3*~7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5*~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.0/0.8/0.6**	W
T <sub>solder</sub>	Soldering Temperature	260·10	°C·sec
T <sub>strg</sub>	Storage Temperature	-55~150	°C
T <sub>opr</sub>	Operating Temperature	0~70	°C

\* : -3.0 V at pulse width 50 ns

\*\* : 0.6 inch 1.0 W, 0.3 inch 0.8 W, 0.45 inch 0.6 W

# TC55257BPL/BFL/BSPL-85L,-10L TC55257BFTL/BTRL-85L,-10L

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	MIN.	MIN.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> + 0.3	
V <sub>IL</sub>	Input Low Voltage	-0.3*	-	0.8	
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	

\* : -3.0 V at pulse width 50 ns

## D.C. and OPERATING CHARACTERISTICS (Ta = 0~70 °C, V<sub>DD</sub> = 5 V ± 10 %)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 ~ V <sub>DD</sub>	-	-	± 1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V	-1.0	-	-	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	4.0	-	-	mA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ V <sub>OUT</sub> = 0 ~ V <sub>DD</sub>	-	-	± 1.0	μA	
I <sub>DDO1</sub>	Operating Current	$\overline{CE} = V_{IL}$ R/W = V <sub>IH</sub> Other Input = V <sub>IH</sub> / V <sub>IL</sub> I <sub>OUT</sub> = 0 mA	t <sub>cycle</sub> = 1 μs	-	10	-	mA
I <sub>DDO2</sub>		$\overline{CE} = 0.2$ V R/W = V <sub>DD</sub> - 0.2 V Other Input = V <sub>DD</sub> - 0.2 V / 0.2 V I <sub>OUT</sub> = 0 mA	t <sub>cycle</sub> = 1 μs	-	5	-	
I <sub>DDs1</sub>	Standby Current	$\overline{CE} = V_{IH}$	-	-	3	mA	
I <sub>DDs2</sub>	Standby Current	$\overline{CE} = V_{DD} - 0.2$ V <sub>DD</sub> = 2.0 V ~ 5.5 V	Ta = 0~70 °C	-	-	30	μA
			Ta = 25 °C	-	-	2	μA

## CAPACITANCE (Ta = 25 °C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	

Note : This parameter periodically sampled is not 100 % tested.

# TC55257BPL/BFL/BSPL-85L,-10L

# TC55257BFTL/BTRL-85L,-10L

## A.C. CHARACTERISTICS (Ta = 0~70 °C, VDD = 5 V ± 10 %)

### Read Cycle

SYMBOL	PARAMETER	TC55257BPL / BFL / BSPL / BFTL / BTRL - 85L		TC55257BPL / BFL / BSPL / BFTL / BTRL - 10L		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	85	–	100	–	ns
t <sub>ACC</sub>	Address Access Time	–	85	–	100	
t <sub>CO</sub>	$\overline{CE}$ Access Time	–	85	–	100	
t <sub>OE</sub>	Output Enable to Output in Valid	–	45	–	50	
t <sub>COE</sub>	Chip Enable ( $\overline{CE}$ ) to Output in Low-Z	10	–	10	–	
t <sub>OEE</sub>	Output Enable to Output in Low-Z	5	–	5	–	
t <sub>OD</sub>	Chip Enable ( $\overline{CE}$ ) to Output in High-Z	–	30	–	50	
t <sub>ODO</sub>	Output Enable to Output in High-Z	–	30	–	40	
t <sub>OH</sub>	Output Data Hold Time	10	–	10	–	

### Write Cycle

SYMBOL	PARAMETER	TC55257BPL / BFL / BSPL / BFTL / BTRL - 85L		TC55257BPL / BFL / BSPL / BFTL / BTRL - 10L		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	85	–	100	–	ns
t <sub>WP</sub>	Write Pulse Width	60	–	70	–	
t <sub>CW</sub>	Chip Selection to End of Write	65	–	90	–	
t <sub>AS</sub>	Address Set up Time	0	–	0	–	
t <sub>WR</sub>	Write Recovery Time	5	–	5	–	
t <sub>ODW</sub>	R/W to Output in High-Z	–	30	–	50	
t <sub>OEW</sub>	R/W to Output in Low-Z	5	–	5	–	
t <sub>DS</sub>	Data Set up Time	40	–	40	–	
t <sub>DH</sub>	Data Hold Time	0	–	0	–	

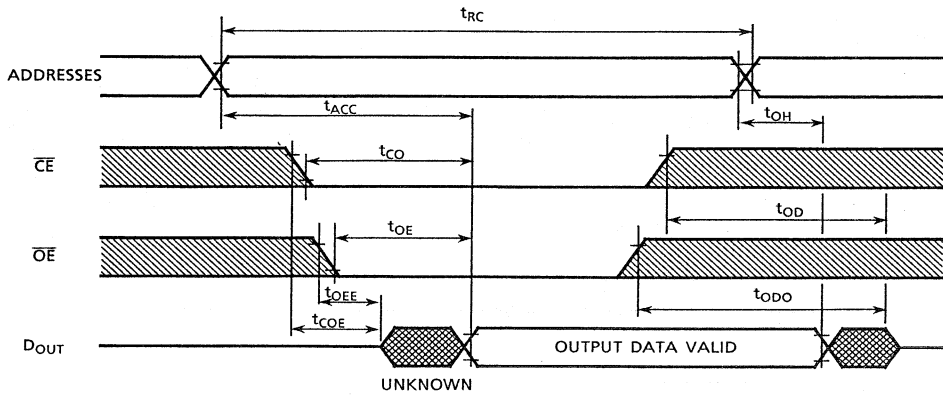
### A.C. Test Conditions

Output Load : 100 pF + 1 TTL Gate  
 Input Pulse Level : 0.6 V, 2.4 V  
 Timing Measurement : 0.8 V, 2.2 V  
 Reference Level : 0.8 V, 2.2 V  
 t<sub>r</sub>, t<sub>f</sub> : 5 ns

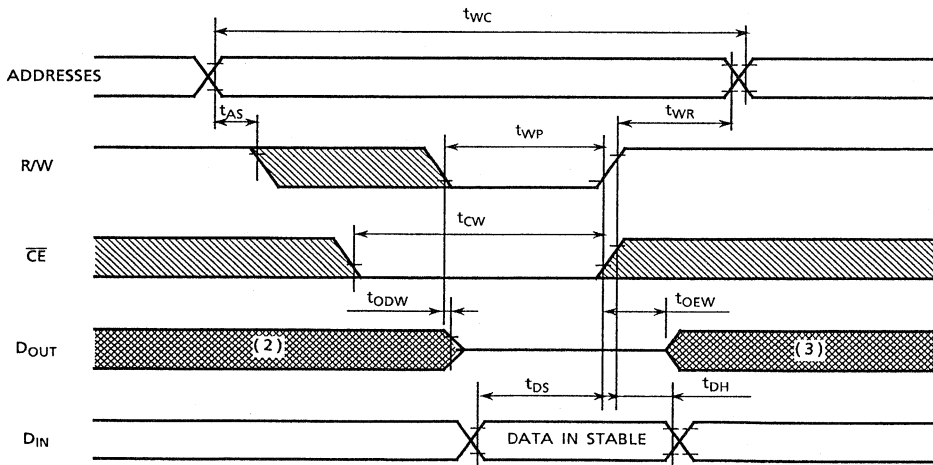
**TC55257BPL/BFL/BSPL-85L,-10L**  
**TC55257BFTL/BTRL-85L,-10L**

**TIMING WAVEFORMS**

**Read Cycle (1)**

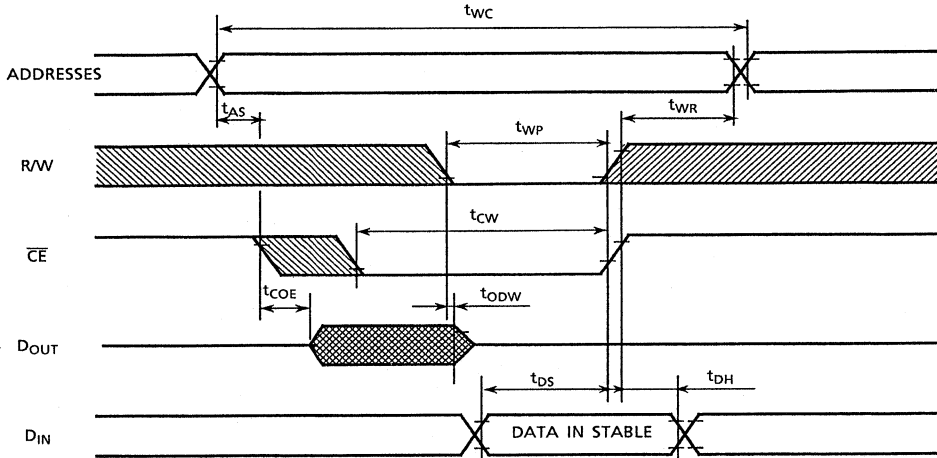


**Write Cycle 1 (4) (R/W Controlled Write)**



**TC55257BPL/BFL/BSPL-85L,-10L**  
**TC55257BFTL/BTRL-85L,-10L**

Write Cycle 2 (4) ( $\overline{\text{CE}}$  Controlled Write)



Note : (1) R/W is High for read cycle.

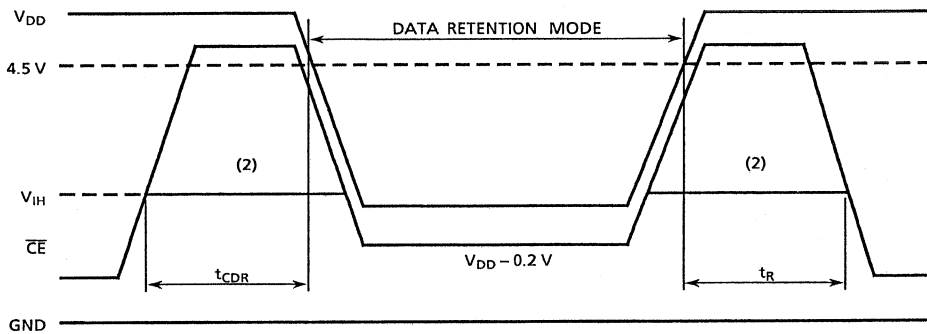
- (2) Assuming that  $\overline{\text{CE}}$  low transition occurs coincident with or after R/W Low transition, Outputs remain a high impedance state.
- (3) Assuming that  $\overline{\text{CE}}$  High transition occurs coincident with or prior to R/W High transition, Outputs remain a high impedance state.
- (4) Assuming that  $\overline{\text{OE}}$  is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS ( $T_a = 0 \sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DH}$	Data Retention Supply Voltage	2.0	-	5.5	V
$I_{DD52}$	Standby Supply Current	$V_{DH} = 3.0\text{ V}$	-	20	$\mu\text{A}$
		$V_{DH} = 5.5\text{ V}$	-	30	
$t_{CDR}$	Chip Deselection to Data Retention Mode	0	-	-	$\mu\text{S}$
$t_R$	Recovery Time	$t_{RC(1)}$	-	-	

Note (1) : Read Cycle Time.

$\overline{\text{CE}}$  Controlled Data Retention Mode



Note (2) : If the  $V_{IH}$  of  $\overline{\text{CE}}$  is 2.2 V in operation,  $I_{DD51}$  current flows during the period that the  $V_{DD}$  voltage is going down from 4.5 V to 2.4 V

**TOSHIBA**

DATA BOOK

**MOS MEMORY**  
(VRAM, SRAM)

**1991**



# INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

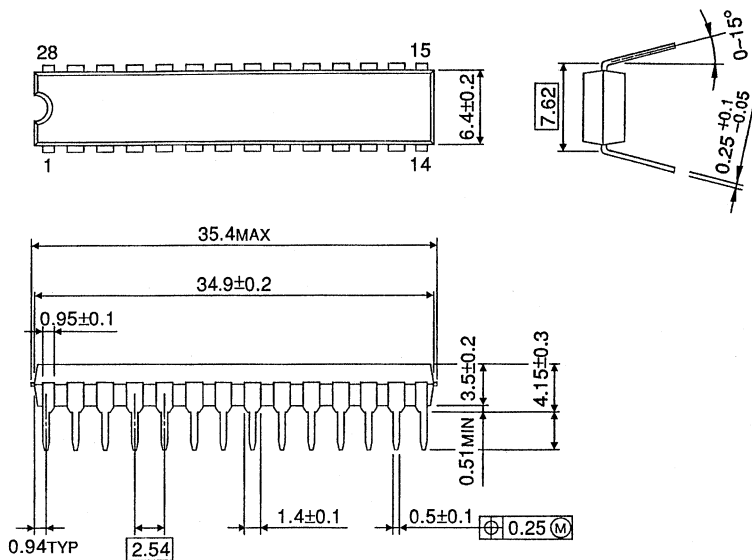
These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

We hope this information will be very useful for you.

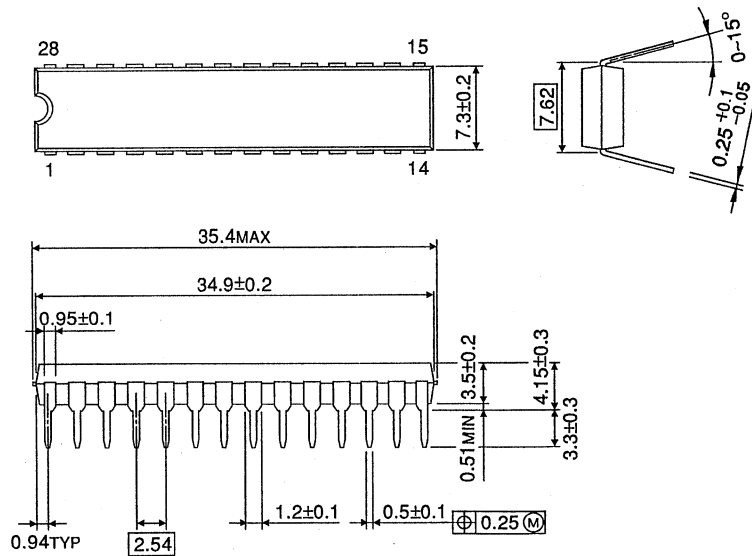
Nov. 1991

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Semiconductor Group

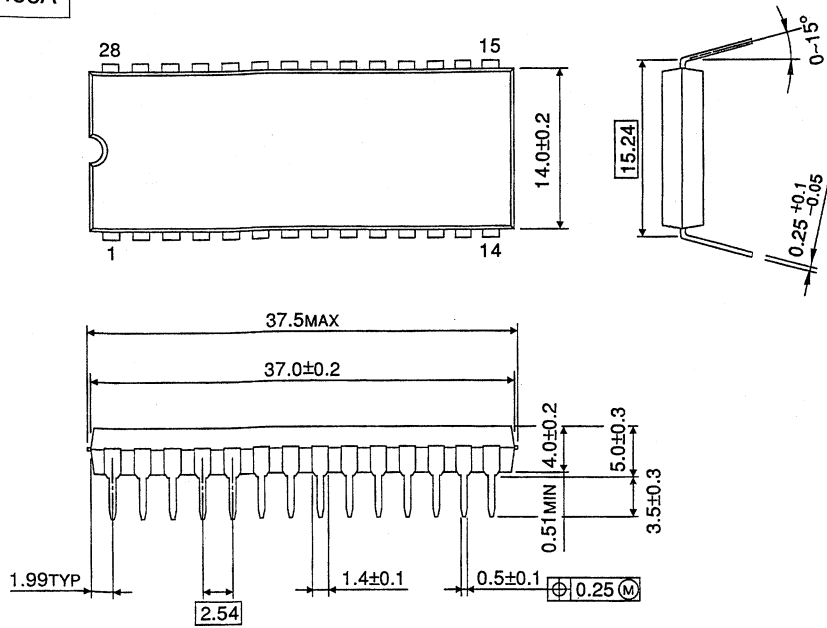
DIP28-P-300A



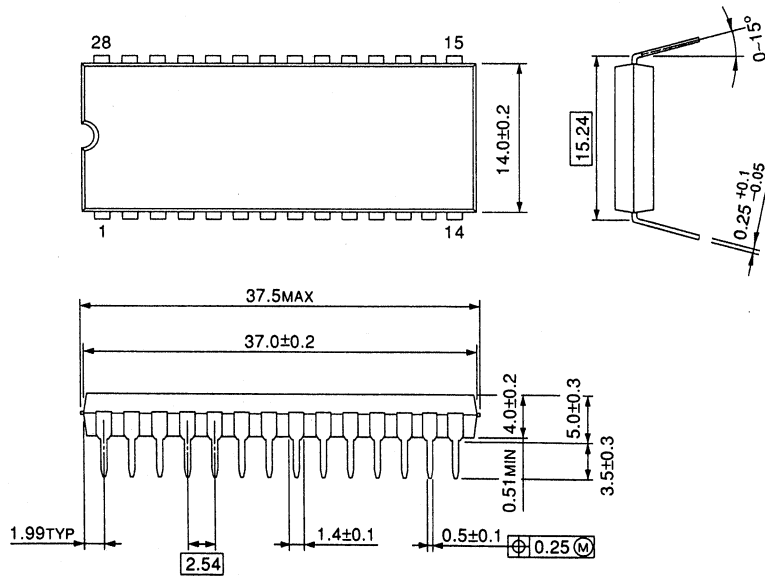
DIP28-P-300B



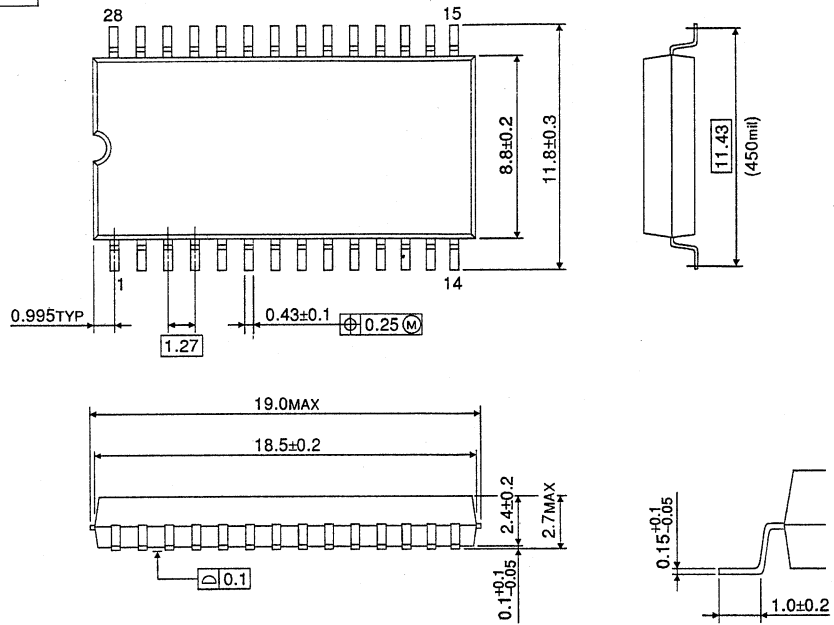
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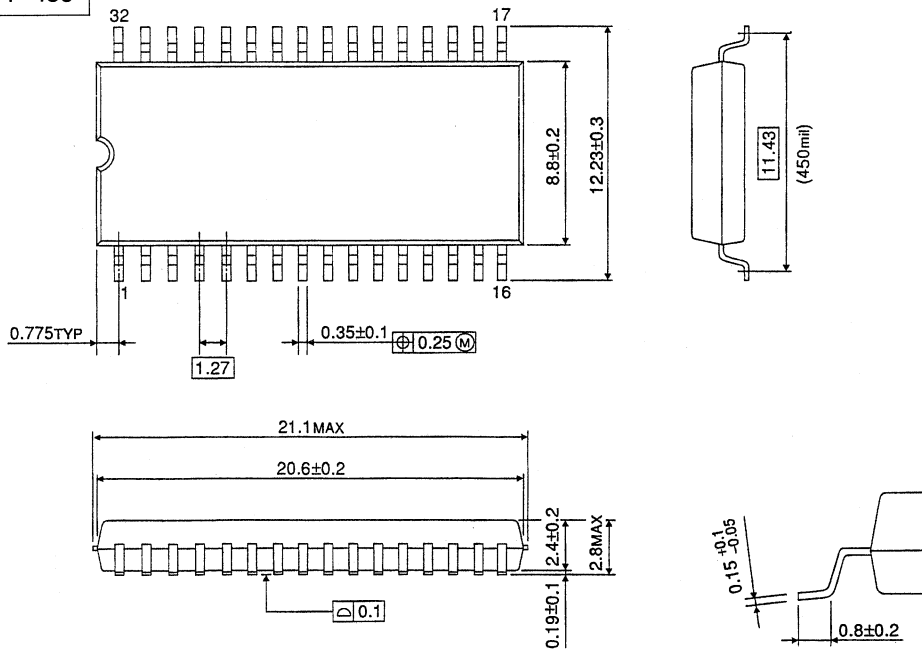
DIP28-P-600



SOP28-P-450

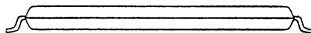
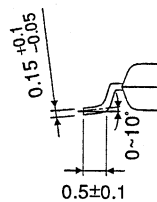
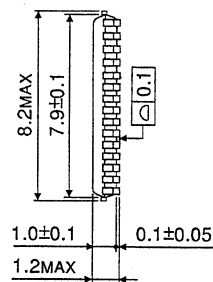
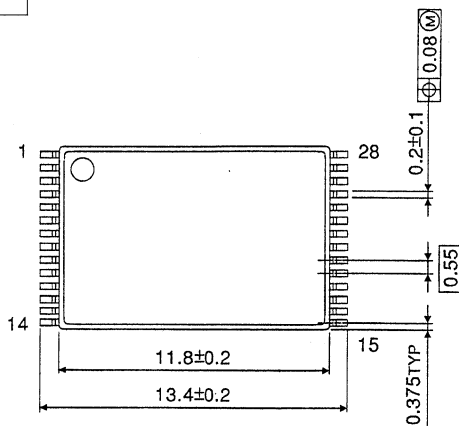


SOP32-P-450



TSOP28-P

TENTATIVE



TSOP28-P-A

TENTATIVE

