

# TC55416P-15H,-20H,-25H,-35H

16,384 WORD × 4 BIT CMOS STATIC RAM

## DESCRIPTION

The TC55416P-H is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 15ns/20ns/25ns/35ns and maximum operating current of 120mA/100mA/100mA/80mA at minimum cycle time.

The TC55416P-H also features an automatic stand-by mode. When deselected by Chip Enable ( $\overline{CE}$ ), the operating current is reduced to 1mA.

The TC55416P is suitable for use in cache memory and high speed storage, where high speed/high density are required.

The TC55416P-H is moulded in a 22 pin standard plastic DIP with 0.3 inch width for high density assembly.

The TC55416P-H is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

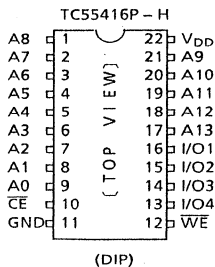
## FEATURES

- Fast access time :
 

TC55416P-15H	15ns(MAX.)
TC55416P-20H	20ns(MAX.)
TC55416P-25H	25ns(MAX.)
TC55416P-35H	35ns(MAX.)
- 5V single power supply : 5V ± 10%
- Fully static operation
- Directly TTL compatible :
  - All Input and Output
- Low power dissipation :
 

Operation	TC55416P-15H	120mA(MAX.)
	TC55416P-20H	100mA(MAX.)
	TC55416P-25H	100mA(MAX.)
	TC55416P-35H	80mA(MAX.)
Standby		1mA(MAX.)
- Package  
TC55416P-H : DIP22-P-300

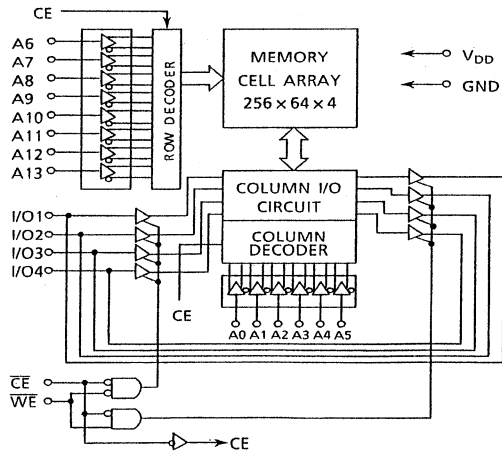
## PIN CONNECTION



## PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Input / Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V <sub>DD</sub>	Power (+ 5V)
GND	Ground

## BLOCK DIAGRAM



## MAXIMUM RATINGS

SYMBOL	CHARACTERISTIC	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.5~7.0	V
V <sub>IN</sub>	Input Voltage	-2.0~7.0	V
V <sub>IO</sub>	Output Voltage	-0.5~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	650	mW
T <sub>solder</sub>	Soldering Temperature · Time	260 · 10	°C·sec
T <sub>strg</sub>	Storage Temperature	-65~150	°C
T <sub>opr</sub>	Operating Temperature	-10~85	°C

## DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	* -3.0	-	0.8	V

\* Pulse width ≤ 10ns, DC : -0.5V (min)

## DC and OPERATING CHARACTERISTICS (T<sub>a</sub> = 0~70°C, V<sub>DD</sub> = 5V ± 10%)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0~V <sub>DD</sub>	-	-	± 1	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-4	-	-	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	8	-	-	mA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , V <sub>OUT</sub> = 0~V <sub>DD</sub>	-	-	± 1	μA	
I <sub>DDO</sub>	Operating Current	V <sub>DD</sub> = 5.5V, tcycle = Min cycle $\overline{CE} = V_{IL}$ , I <sub>OUT</sub> = 0mA Other Input = V <sub>IH</sub> / V <sub>IL</sub>	- 15H	-	-	120	mA
			- 20H	-	-	100	
			- 25H	-	-	100	
			- 35H	-	-	80	
I <sub>DD5 1</sub>	Standby Current	V <sub>DD</sub> = 5.5V, tcycle = Min cycle $\overline{CE} = V_{IH}$ , Other Input = V <sub>IH</sub> / V <sub>IL</sub>	-	-	25	mA	
I <sub>DD5 2</sub>		$\overline{CE} = V_{DD} - 0.2V$ Other Input = V <sub>DD</sub> - 0.2V or 0.2V	-	-	1		

## CAPACITANCE (T<sub>a</sub> = 25°C)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	7	pF

NOTE : This parameter periodically sampled is not 100% tested.

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AC CHARACTERISTICS (Ta=0~70°C<sup>(4)</sup>, VDD=5V±10%)

## READ CYCLE

SYMBOL	CHARACTERISTIC	TC55416P - 15H		TC55416P - 20H		TC55416P - 25H		TC55416P - 35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	15	-	20	-	25	-	35	-	ns
t <sub>ACC</sub>	Address Access Time	-	15	-	20	-	25	-	35	
t <sub>CO</sub>	Chip Enable Access Time	-	15	-	20	-	25	-	35	
t <sub>COE</sub>	Output Enable Time from $\overline{CE}$	5	-	5	-	5	-	5	-	
t <sub>COD</sub>	Output Disable Time from $\overline{CE}$	-	6	-	6	-	6	-	6	
t <sub>OH</sub>	Output Data Hold Time	5	-	5	-	5	-	5	-	
t <sub>PU</sub>	Power Up Time	0	-	0	-	0	-	0	-	
t <sub>PD</sub>	Power Down Time	-	15	-	20	-	25	-	35	

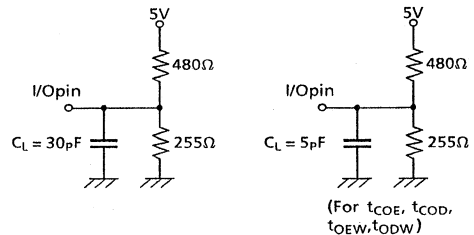
## WRITE CYCLE

SYMBOL	CHARACTERISTIC	TC55416P - 15H		TC55416P - 20H		TC55416P - 25H		TC55416P - 35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	15	-	20	-	25	-	35	-	ns
t <sub>WP</sub>	Write Pulse Width	12	-	13	-	13	-	13	-	
t <sub>CW</sub>	Chip Enable to End of Write	12	-	13	-	13	-	13	-	
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	0	-	0	-	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	0	-	
t <sub>OE<sub>W</sub></sub>	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	0	-	
t <sub>OD<sub>W</sub></sub>	Output Disable Time from $\overline{WE}$	-	6	-	6	-	6	-	6	
t <sub>DS</sub>	Data Set Up Time	9	-	10	-	10	-	10	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	0	-	

## AC TEST CONDITIONS

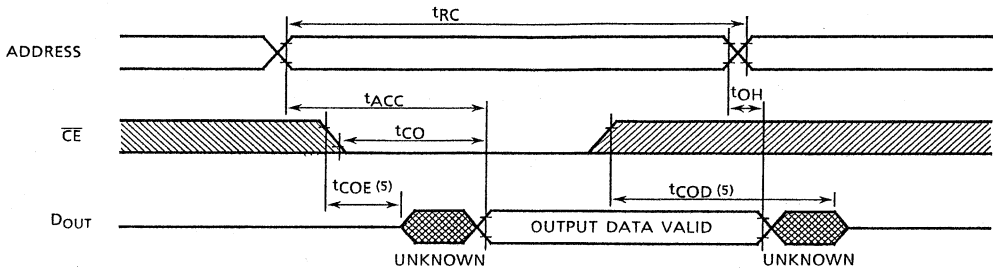
Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	See Fig. 1

Fig. 1

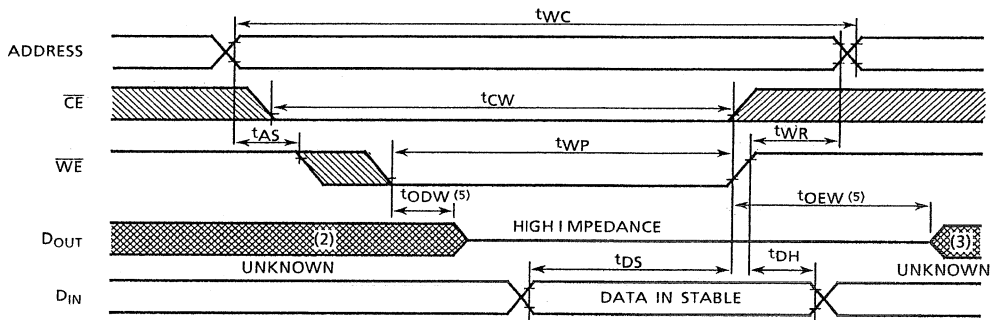


TIMING WAVEFORMS

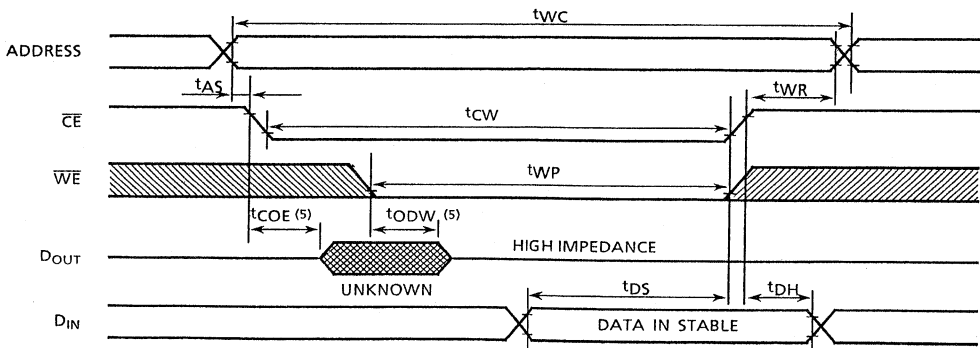
READ CYCLE <sup>(1)</sup>



WRITE CYCLE 1 ( $\overline{WE}$  Controlled Write)



WRITE CYCLE 2 ( $\overline{CE}$  Controlled Write)

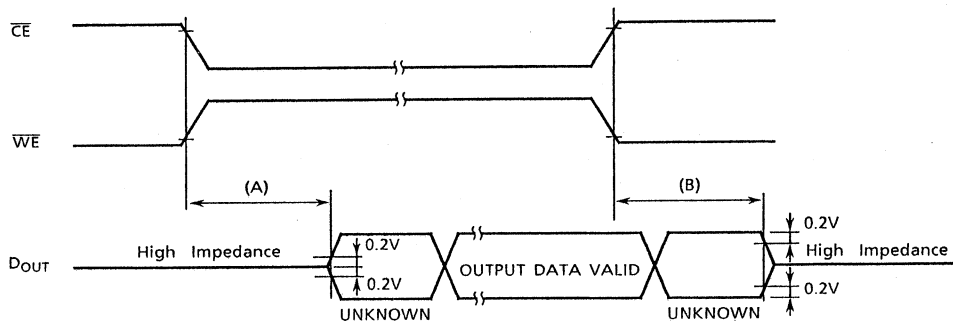


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- (注) 1.  $\overline{WE}$  is High for Read Cycle.
2. Assuming that  $\overline{CE}$  Low transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
  3. Assuming that  $\overline{CE}$  High transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
  4. The Operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
  5. These parameters are specified as follows and measured by using the load shown in Fig.1.

(A)  $t_{COE}, t_{OEw}$  ..... Output Enable Time

(B)  $t_{COD}, t_{ODW}$  ..... Output Disable Time



**TOSHIBA**

DATA BOOK

**MOS MEMORY**  
(VRAM, SRAM)

**1991**

# INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

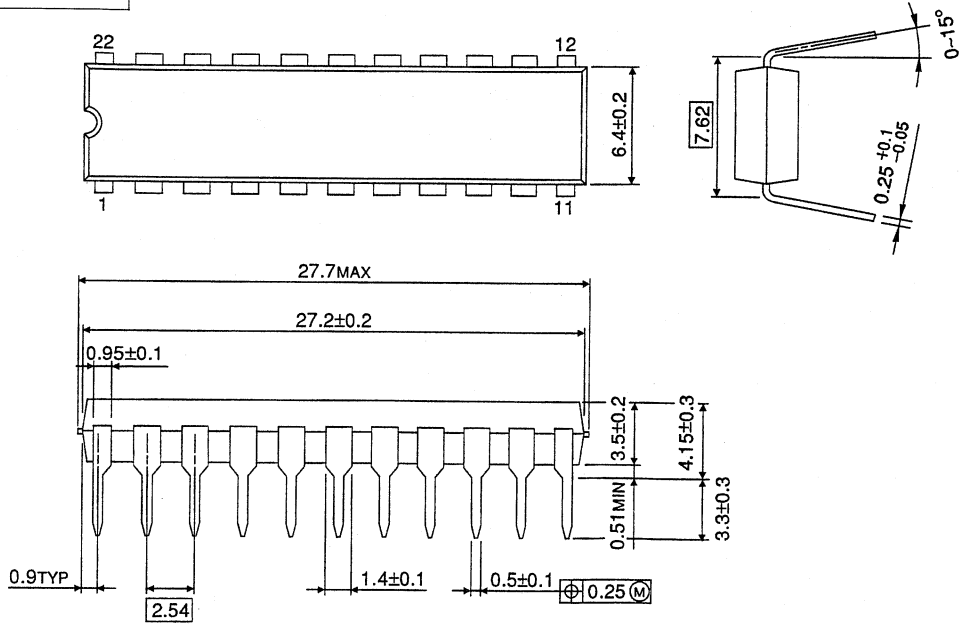
We hope this information will be very useful for you.

Nov. 1991

TOSHIBA CORPORATION  
Semiconductor Group

Unit in mm

### DIP22-P-300



### DIP24-P-300B

