TC55417P/J-15H,-20H,-25H,-35H

16,384 WORD × 4 BIT CMOS STATIC RAM

DESCRIPTION

The TC55417P/J−H is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated form a single 5 - volt supply. Toshiba's high performance device technolgy provides both high speed and low power features with a maximum access time of 15ns / 20ns / 25ns / 35ns and maximum operating current of 120mA / 100mA / 100mA / 80mA at minimum cycle time.

The TC55417P/J−H also features an automatic stand - by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 1mA.

The TC55417P/J−H is suitable for use in cache memory and high speed storage, where high speed / high density are required.

The TC55417P/J−H is moulded in a 24 pin standard plastic DIP and a 24 pin plastic SOJ, with 0.3 inch width for high density assembly.

The TC55417P/J−H is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time :

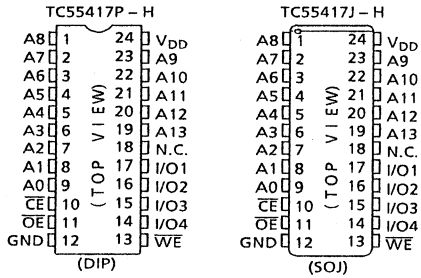
TC55417P/J−15H	15ns(MAX.)
TC55417P/J−20H	20ns(MAX.)
TC55417P/J−25H	25ns(MAX.)
TC55417P/J−35H	35ns(MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- Diractly TTL compatible :
  All Input and Output
- Low power dissipation :

Operation	TC55417P/J−15H	120mA(MAX.)
	TC55417P/J−20H	100mA(MAX.)
	TC55417P/J−25H	100mA(MAX.)
	TC55417P/J−35H	80mA(MAX.)
Standby		1mA(MAX.)

- Outpot buffer control : $\overline{OE}$
- Package
  TC55417P−H : DIP24−P−300B
  TC55417J−H : SOJ24−P−300A

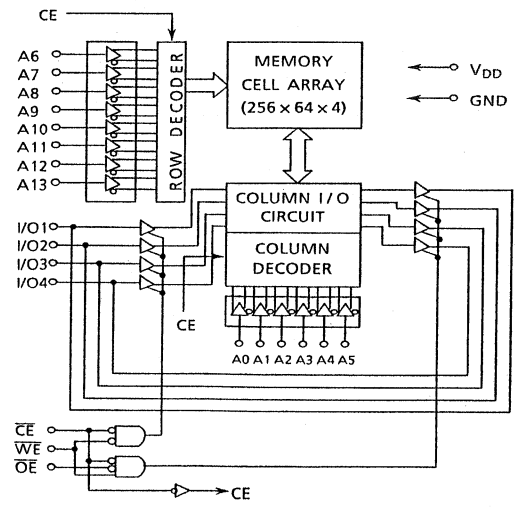
PIN CONNECTION



PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Input / Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+ 5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD} + 0.5	V
P_D	Power Dissipation	650	mW
Tsolder	Soldering Temperature · Time	260 · 10	°C · sec
Tstrg	Storage Temperature	−65~150	°C
Topr	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	* − 3.0	−	0.8	V

* Pulse width ≦ 10ns, DC : −0.5V (min)

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		−	−	± 1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		− 4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0~V_{DD}		−	−	± 1	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V, tcycle = Min cycle $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA Other Input = V_{IH} / V_{IL}	− 15H	−	−	120	mA
			− 20H	−	−	100	
			− 25H	−	−	100	
			− 35H	−	−	80	
I_{DDS1}	Standby Current	V_{DD} = 5.5V, tcycle = Min cycle $\overline{CE}$ = V_{IH}, Other Input = V_{IH} / V_{IL}		−	−	25	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Input = V_{DD} − 0.2V or 0.2V		−	−	1	

CAPACITANCE (Ta = 25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	7	pF

Note : This parameter periodically sampled is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C [4], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55417P/J-15H		TC55417P/J-20H		TC55417P/J-25H		TC55417P/J-35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	–	35	ns
t_{CO}	Chip Enable Access Time	–	15	–	20	–	25	–	35	ns
t_{OE}	Output Enable to Output Valid	–	9	–	10	–	10	–	10	ns
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	5	–	ns
t_{COD}	Output Disable Time from $\overline{CE}$	–	6	–	6	–	6	–	6	ns
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	0	–	0	–	0	–	ns
t_{ODO}	Output Disable Time from $\overline{OE}$	–	5	–	5	–	5	–	5	ns
t_{OH}	Output Data Hold Time	5	–	5	–	5	–	5	–	ns
t_{PU}	Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Power Down Time	–	15	–	20	–	25	–	35	ns

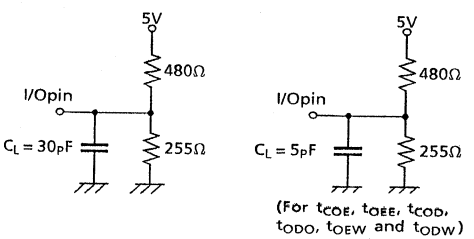
WRITE CYCLE

SYMBOL	PARAMETER	TC55417P/J-15H		TC55417P/J-20H		TC55417P/J-25H		TC55417P/J-35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	ns
t_{WP}	Write Pulse Width	12	–	13	–	13	–	13	–	ns
t_{CW}	Chip Enable to End of Write	12	–	13	–	13	–	13	–	ns
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	ns
t_{ODW}	Output Disable Time from $\overline{WE}$	–	6	–	6	–	6	–	6	ns
t_{DS}	Data Set Up Time	9	–	10	–	10	–	10	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns

AC TEST CONDITIONS

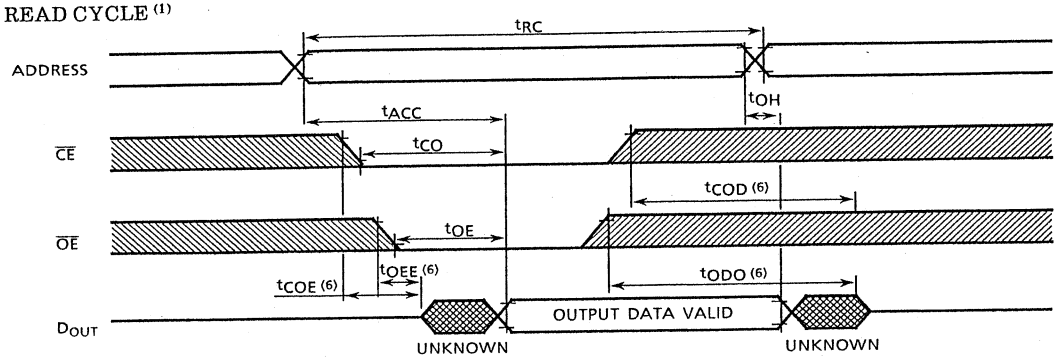
Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	See Fig. 1

Fig. 1

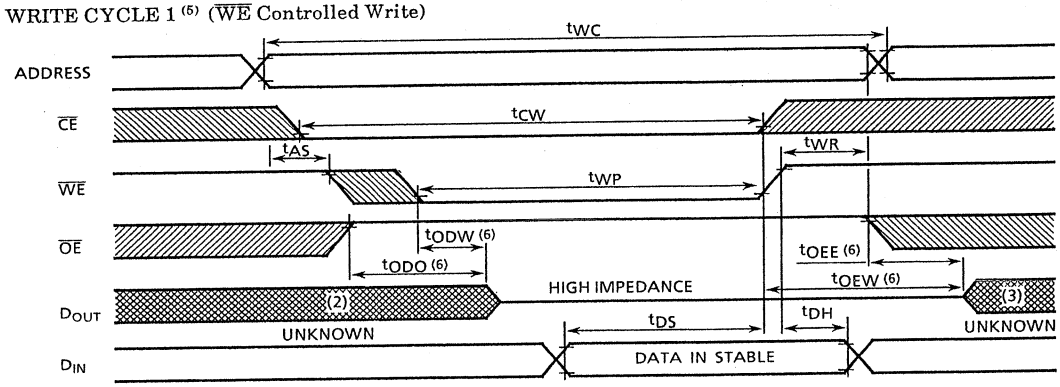


TIMING WAVEFORMS

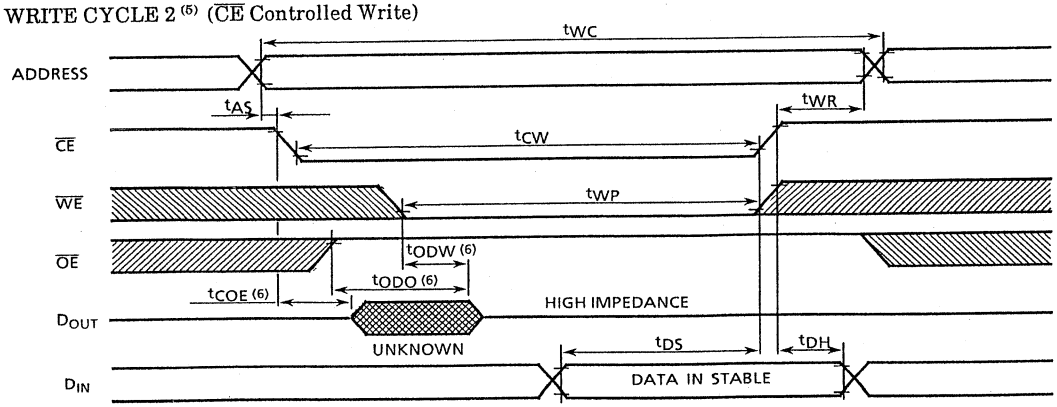
READ CYCLE (1)



WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE}$ Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occures coincident with or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.

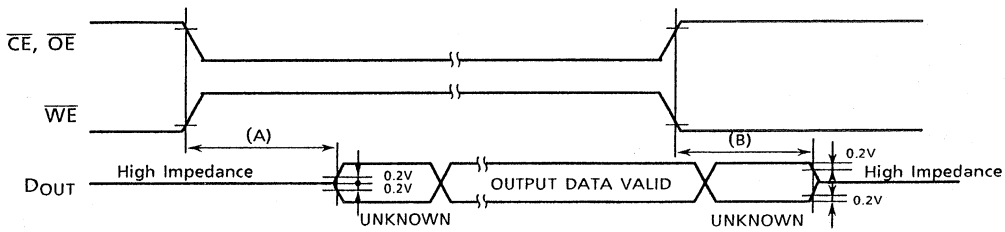
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

5. The $\overline{OE}$ input can be held on low (V_{IL}) in write cycle.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

   (B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

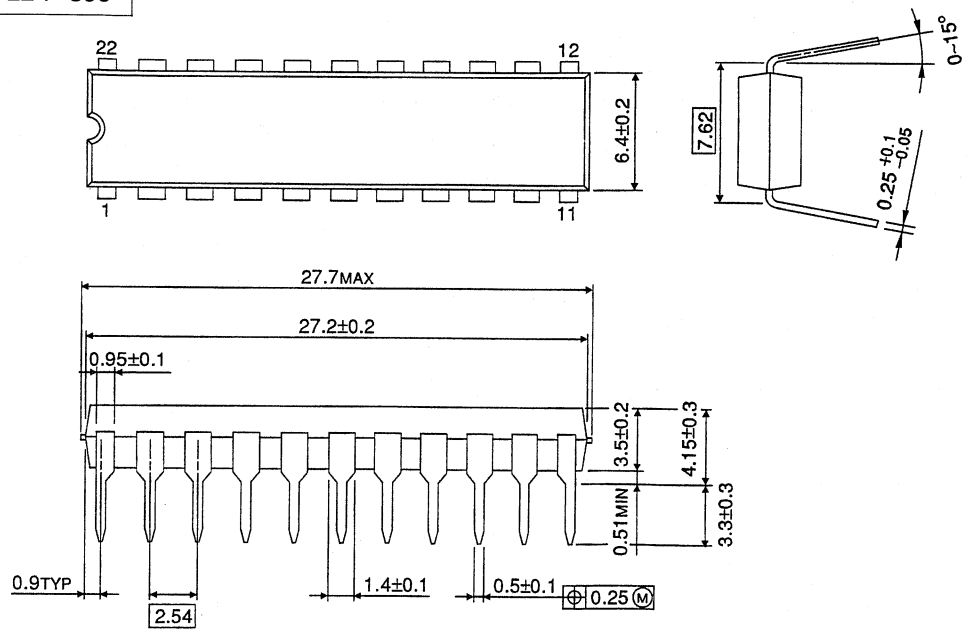
We hope this information will be very useful for you.

Nov. 1991

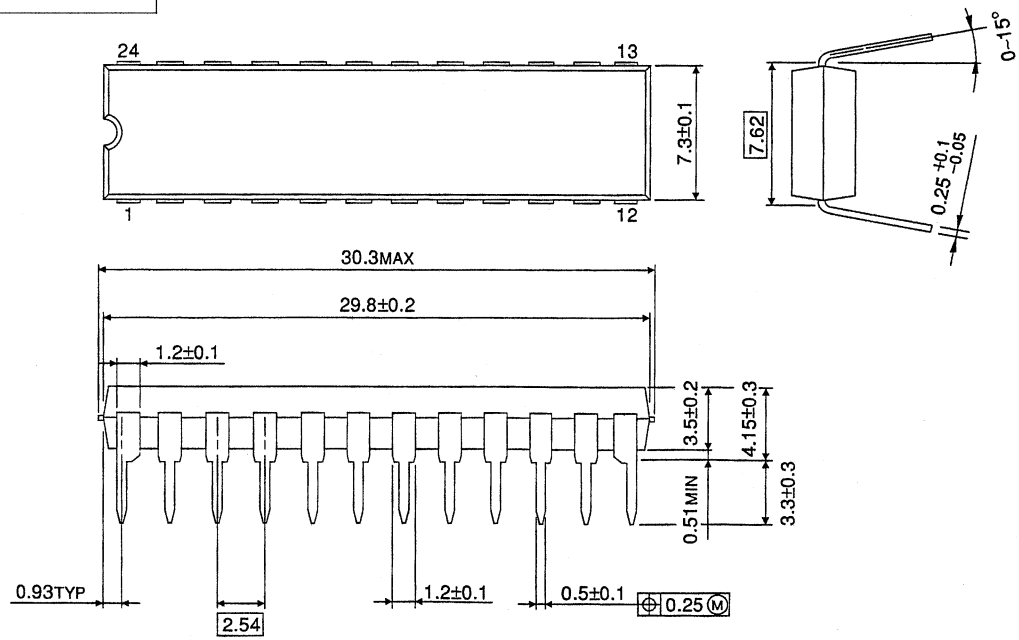
TOSHIBA CORPORATION
Semiconductor Group

Unit in mm

DIP22-P-300

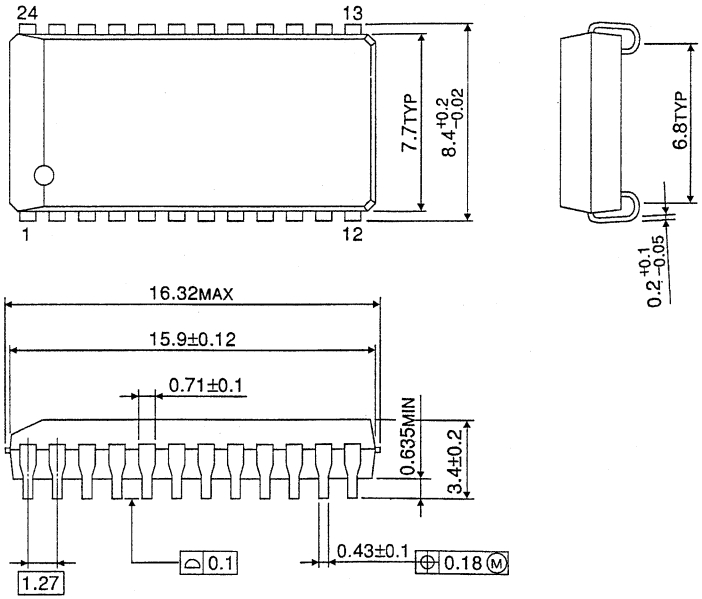


DIP24-P-300B



Unit in mm

SOJ24-P-300



SOJ24-P-300A