TC5563APL-10,-12,-15

8,192 WORD 8 BIT CMOS STATIC RAM

DESCRIPTION

The TC5563APL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates froma single 5V supply. Advanced circuit technique provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE2 is a logical low or $\overline{CE1}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5563APL has three control inputs. Two chip enable ($\overline{CE1}$, CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5563APL is suitable for use in various microprocessor application system where high speed, low power, and battery back up are required.

The TC5563APL also features pin compatibility with the 64K bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems. The TC5563APL is offered in a dual-in-line 28 pin standard 300 mil plastic package.

FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current: 100μA(Max.) Ta=70°C
- Access Time
  TC5563APL-10: 100ns(Max.)
  TC5563APL-12: 120ns(Max.)
  TC5563APL-15: 150ns(Max.)
- 5V Single Power Supply
- Power Down Features: CE2, $\overline{CE1}$
- Fully Static Operation
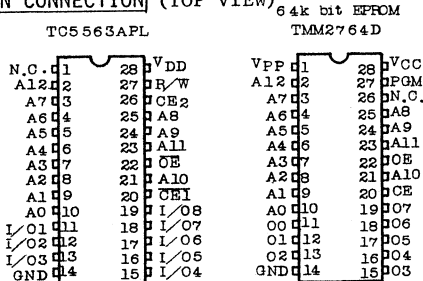- Data Retention Supply Voltage: 2.0∿5.5V

- Directly TTL Compatible: All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package type)

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package (SOP)	*TC5565AFL

*: See TC5565APL/AFL Technical Data.
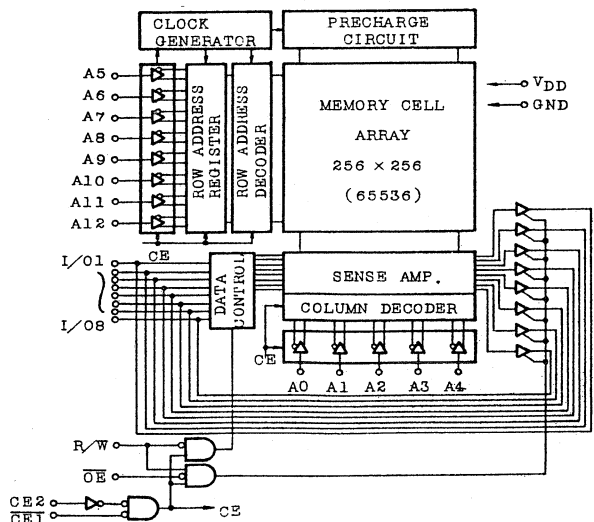
- Package : TC5563APL : DIP28-P-300B

PIN CONNECTION (TOP VIEW)

64k bit EPROM

TC5563APL

N.C.	1	28	V_{DD}
A12	2	27	R/W
A7	3	26	CE2
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{OE}$
A2	8	21	A10
A1	9	20	$\overline{CE1}$
A0	10	19	I/O8
I/O1	11	18	I/O7
I/O2	12	17	I/O6
I/O3	13	16	I/O5
GND	14	15	I/O4

TMM2764D

VPP	1	28	VCC
A12	2	27	PGM
A7	3	26	N.C.
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE
A2	8	21	A10
A1	9	20	CE
A0	10	19	O7
O0	11	18	O6
O1	12	17	O5
O2	13	16	O4
GND	14	15	O3

PIN NAMES

A0 ∿ A12	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ∿ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM

OPERATION MODE

OPEPATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/01∿I/08	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3∿7.0	V
V_{IN}	Input Voltage	−0.3*∿7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5∿V_{DD}+0.5	V
P_D	Power Dissipation	0.8	W
T_{solder}	Soldering Temperature	260·10	°C·sec
T_{stg}	Storage Tememprature	−55∿150	°C
T_{opr}	Operating Temperature	0∿70	°C

*: −3.0V at pulse width 50ns Max.

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.3	
V_{IL}	Input Low Voltage	−0.3*	−	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	

*: −3.0V at pulse width 50ns Max.

D.C. and OPERATING CHARACTERISTICS (Ta=0∿70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0∿V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			–1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			4.0	–	–	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or R/W=V_{IL} or $\overline{OE}$=V_{IH} V_{OUT}=0∿V_{DD}			–	–	±1.0	μA
I_{DDO1}	Operating Current	V_{DD}=5.5V $\overline{CE1}$=V_{IL} CE2=V_{IH} Other input= V_{IH}/V_{IL} I_{OUT}=0mA	t_{cycle}=1.0μs		–	–	10	mA
			TC5563APL-10	t_{cycle}=100ns	–	–	45	mA
			TC5563APL-12	t_{cycle}=120ns	–	–	40	mA
			TC5563APL-15	t_{cycle}=150ns	–	–	35	mA
I_{DDO2}		V_{DD}=5.5V $\overline{CE1}$=0.2V CE2=V_{DD}-0.2V Other input= V_{DD}-0.2V/0.2V I_{OUT}=0mA	t_{cycle}=1.0μs		–	–	5	mA
			TC5563APL-10	t_{cycle}=100ns	–	–	40	mA
			TC5563APL-12	t_{cycle}=120ns	–	–	35	mA
			TC5563APL-15	t_{cycle}=150ns	–	–	30	mA
I_{DDS1}	Standby Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL}			–	–	3	mA
* I_{DDS2}	Standby Current	$\overline{CE1}$=V_{DD}-0.2V or CE2=0.2V	V_{DD}=5.5V		–	2	100	μA
			V_{DD}=3.0V		–	1	50	

*: In standby mode with $\overline{CE1}\geqq V_{DD}$-0.2V, these specification limits are guaranteed under the condition of CE2$\geqq V_{DD}$-0.2V or CE2$\leqq$0.2V.

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ~ 70°C, V_{DD}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	–	120	–	150	–	
t_{ACC}	Address Access Time	–	100	–	120	–	150	
t_{CO1}	$\overline{CE1}$ Access Time	–	100	–	120	–	150	
t_{CO2}	CE2 Access Time	–	100	–	120	–	150	
t_{OE}	Output Enable to Output Valid	–	50	–	60	–	70	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	–	10	–	15	–	ns
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	35	–	40	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	35	–	40	–	50	
t_{OH}	Output Data Hold Time	20	–	20	–	20	–	

WRITE CYCLE

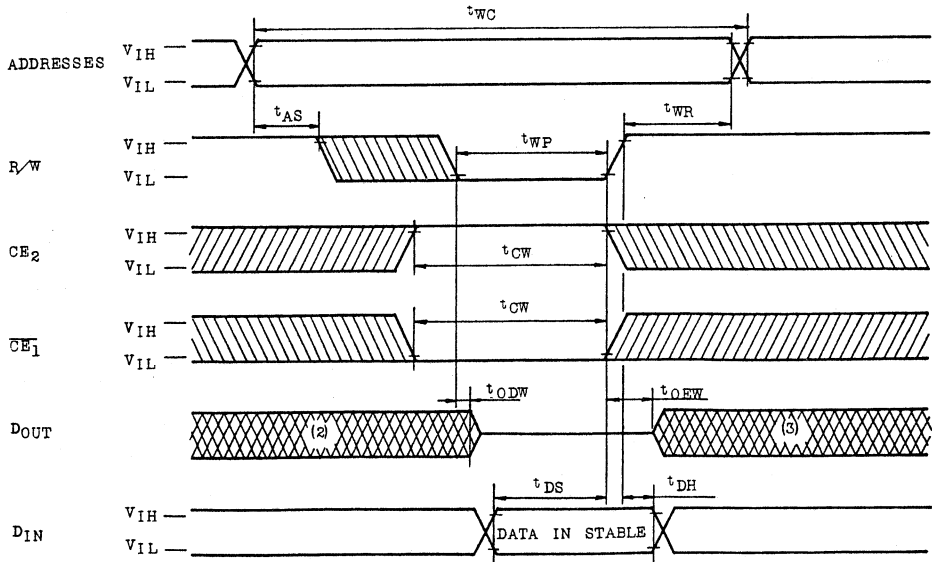| SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	–	120	–	150	–	
t_{WP}	Write Pulse Width	60	–	70	–	90	–	
t_{CW}	Chip Selection to End of Write	80	–	85	–	100	–	
t_{AS}	Address Set up Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{ODW}	R/W to Output High-Z	–	35	–	40	–	50	
t_{OEW}	R/W to Output Low-Z	5	–	5	–	10	⌐	
t_{DS}	Data Set up Time	40	–	50	–	60	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

A.C. TEST CONDITION

```
Output Load           : 100pF + 1 TTL Gate
Input Pulse Level     : 0.6V, 2.4V
Timing Measurement    V_IN : 0.8V, 2.2V
Reference Level       V_OUT: 0.8V, 2.2V
t_r, t_f              : 5ns
```
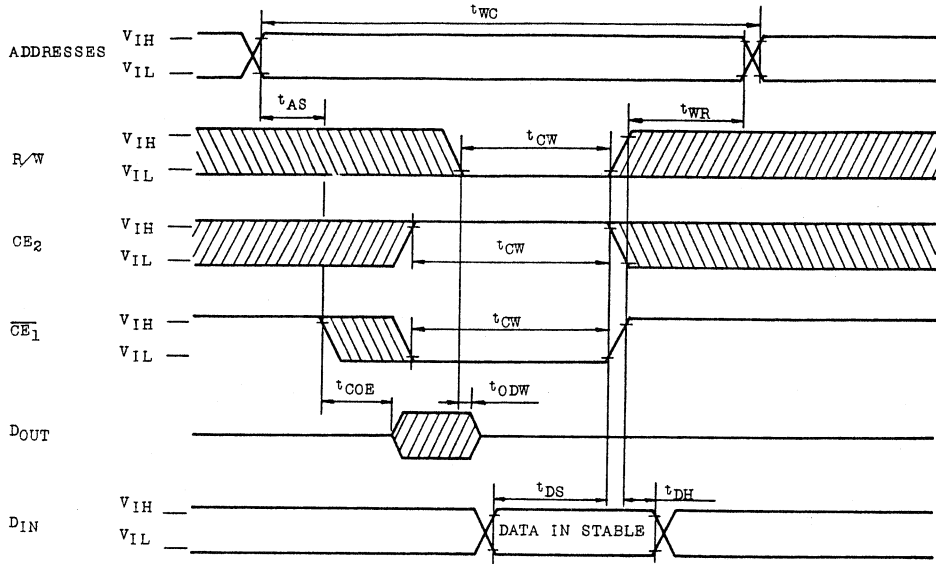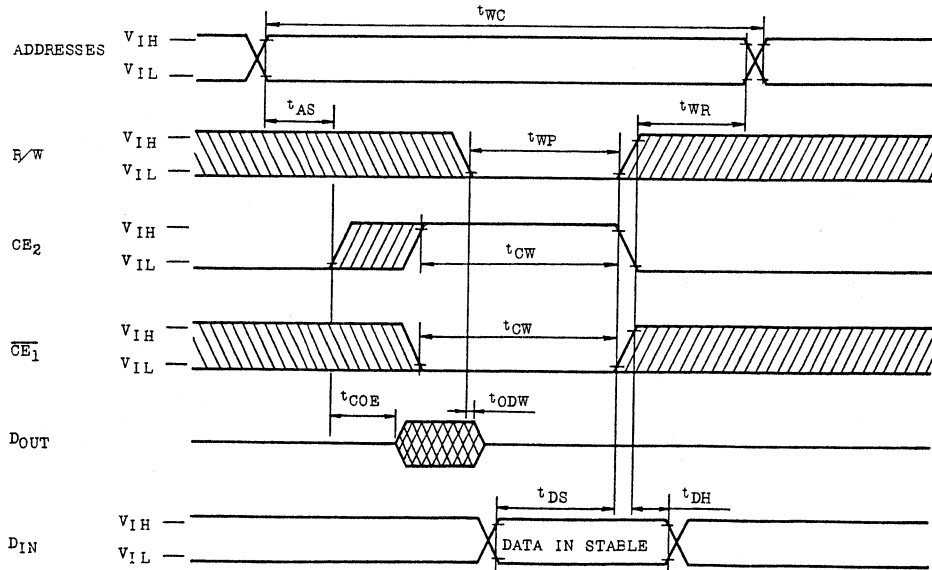
TIMING WAVEFORMS

READ CYCLE (1)

WRITE CYCLE 1 (4)　(R/W Controlled Write)

WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)

WRITE CYCLE 3 (4) (CE2 Controlled Write)
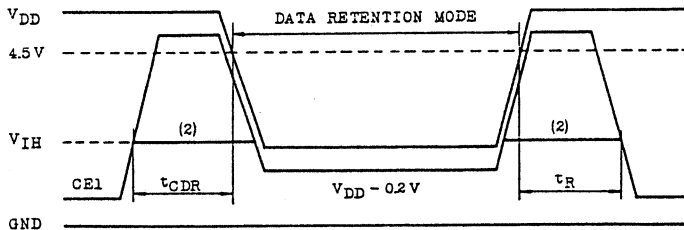
Note 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CEI}$ Low transition of CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CEI}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

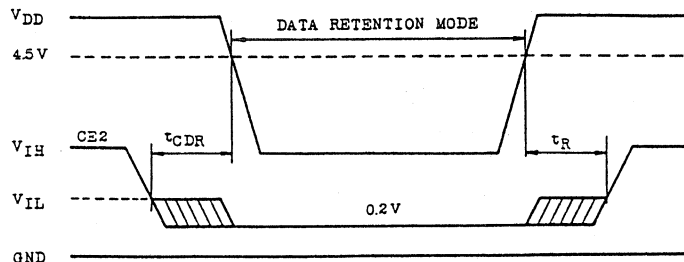DATA RETENTION CHARACTERISTICS   (Ta=0 ～ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Stand by Supply Current	V_{DD}=3.0V	–	–	50	μA
		V_{DD}=5.5V	–	–	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	–	–	μs
t_R	Recovery Time		t_{RC} *			

*: Read cycle time.

$\overline{CEI}$ Controlled Data Retention Mode (1)

CE2 Controlled Data Retention Mode (3)

Note 1: In $\overline{CEI}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V or CE2 $\geqq$ V_{DD}-0.2V.

2: If the V_{IH} of $\overline{CEI}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

3: In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V.

DEVICE INFORMATION

The TC5563APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.
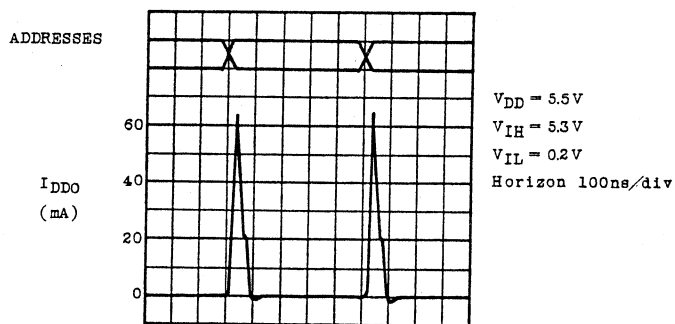
ADDRESSES

I_{DDO}
(mA)

60
40
20
0

V_{DD} = 5.5 V
V_{IH} = 5.3 V
V_{IL} = 0.2 V
Horizon 100ns/div

Fig. Typical Current Waveforms

TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.
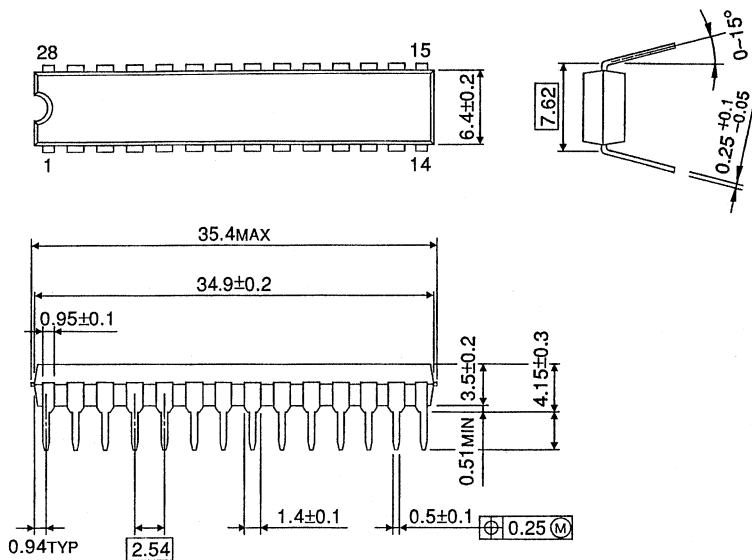
These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

We hope this information will be very useful for you.

Nov. 1991

TOSHIBA CORPORATION
Semiconductor Group

DIP28-P-300A

28   15
1   14

6.4±0.2

7.62

0~15°

0.25 +0.1 -0.05

35.4MAX

34.9±0.2

0.95±0.1

3.5±0.2

4.15±0.3

0.51MIN

1.4±0.1   0.5±0.1

⊕ 0.25 Ⓜ

0.94TYP   2.54

DIP28-P-300B

28   15
1   14

7.3±0.2

7.62

0~15°

0.25 +0.1 -0.05

35.4MAX

34.9±0.2

0.95±0.1

3.5±0.2

4.15±0.3

3.3±0.3

0.51MIN

1.2±0.1   0.5±0.1

⊕ 0.25 Ⓜ

0.94TYP   2.54