SILICON GATE CMOS DIGITAL INTEGRATED CIRCUIT

TC5564APL/AFL-15,-20

8,192 WORD x 8 BIT CMOS STATIC RAM

DESCRIPTION

TC5564APL is 65536 bits static random access memory organized as 8192 words by 8 bits using CMOS technology, and operates with a single 5V power supply.

Advanced circuit techniques provides low power feature with a maximum operating current of 5mA/MHz. Operation current depends on cycle time.

TC5564APL has three control inputs. Two chip enables ($\overline{CE1}$, CE2) allow for device selection and data retention control. Output enable ($\overline{OE}$) input provides fast memory access. When device is placed in standby mode with chip off state, standby current is typically 0.01μA. So the TC5564APL is suitable for use in various microprocessor application systems where low power and battery back up are required. Ultra low standby power allow not only battery but capacitance backup.

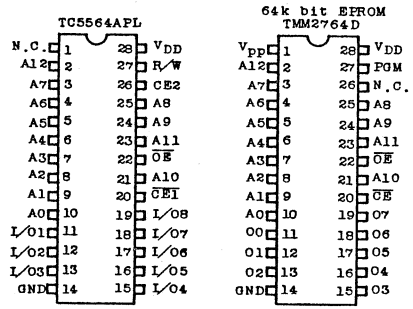
Pin assignment of TC5564APL is pin-compatible with the 64K bits EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

TC5564APL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

FEATURES

- Low Power Dissipation:
  27.5mW/MHz Operating
- Standby Current
  0.2μA (MAX.) at Ta=25°C
  1.0μA (MAX.) at Ta=60°C
- 5V Single Power Supply
- Fully Static Operation
- Data Retention Voltage: 2.0 ~ 5.5V
- Package : TC5564APL : DIP28-P-600
  TC5564AFL : SOP28-P-450
- Pin Compatible with 2764 type EPROM

PIN CONNECTION (TOP VIEW)



PIN NAMES

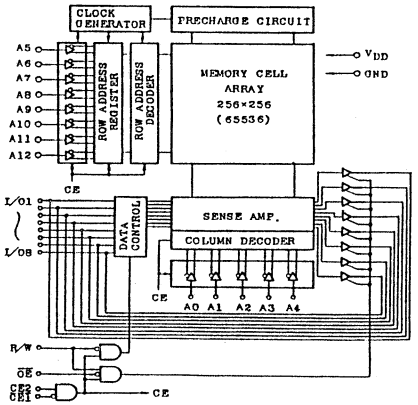
A0 ~ A12	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

- Access Time

	TC5564APL-15 TC5564AFL-15	TC5564APL-20 TC5564AFL-20
Address Access Time (MAX.)	150ns	200ns
$\overline{CE1}$ Access Time (MAX.)	150ns	200ns
CE2 Access Time (MAX.)	150ns	200ns
$\overline{OE}$ Access Time (MAX.)	70ns	100ns

- Directly TTL Compatible: All Inputs and Outputs
- Wide Temperature Operation: -40 ~ 85°C

BLOCK DIAGRAM



OPERATING MODE

Operation Mode	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	Power
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	
Output Deselect	*	*	H	*	High-Z	
Standby	H	*	*	*	"	I_{DDS}
	*	L	*	*	"	I_{DDS}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	
V_{DD}	Power Supply Voltage	-0.3 ∿ 7.0*	V	* 8.5V at 100nS
V_{IN}	Input Voltage	-0.3* ∿ V_{DD}	V	* -3V Pulse Width 50nS
$V_{I/O}$	Input and Output Voltage	-0.5 ∿ V_{DD}+0.5	V	
P_D	Power Dissipation	1.0(0.6)*	W	* SOP
T_{solder}	Soldering Temperature	260 • 10	°C • sec	
T_{stg}	Storage Temperature	-55 ∿ 150	°C	
T_{opr}	Operating Temperature	-40 ∿ 85	°C	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=-40 ∿ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V	
V_{IL}	Input Low Voltage	-0.3*	-	0.8	V	* -3V Pulse Width 50nS
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V	

D.C. and OPERATING CHARACTERISTICS (Ta=-40 ∿ 85°C, V_{DD}=5V±10% Unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Lekage Current	V_{IN}=0 ∿ V_{DD}			-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			-1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			4.0	-	-	mA
V_{OH}	Output High Voltage	I_{OH}=-20μA			V_{DD}-0.1	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=20μA			-	-	0.1	V
I_{LO}	Output Leakage Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or R/W=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0 ∿ V_{DD}			-	-	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$=V_{IL} and CE2=V_{IH}, Other Input=V_{IH}/V_{IL}, I_{OUT}=0mA duty 100%	t_{cycle}=1μs		-	-	10	mA
			MIN CYCLE	TC5564APL-15 TC5564AFL-15	-	-	40	
				TC5564APL-20 TC5564AFL-20	-	-	35	
I_{DDO2}	Operating Current	$\overline{CE1}$=0.2V and CE2=V_{DD}-0.2V, Other Input=V_{DD}-0.2V/0.2V, I_{OUT}=0mA duty 100%	t_{cycle}=1μs		-	-	5	mA
			MIN CYCLE	TC5564APL-15 TC5564AFL-15	-	-	35	
				TC5564APL-20 TC5564AFL-20	-	-	30	
I_{DDS1}	Standby Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL}			-	-	2	mA
I_{DDS2}	Standby Current	$\overline{CE1}$=V_{DD}-0.2V or CE2=0.2V, V_{DD}=2.0 ∿ 5.5V		Ta=25°C	-	0.01	0.2	μA
				Ta=60°C	-	-	1.0	

Note: (1) In standby mode with $\overline{CE1} \geqq V_{DD}$-0.2V, those specification limits are guaranteed under the condition of CE2 ≧ V_{DD}-0.2V or CE2 ≦ 0.2V.
(2) All voltage is measured from GND.

CAPACITANCE (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=-40 ~ 85°C, V_{DD}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TC5564APL-15 TC5564AFL-15		TC5564APL-20 TC5564AFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	-	200	-	ns
t_{ACC}	Address Access Time	-	150	-	200	
t_{CO1}	$\overline{CE1}$ Access Time	-	150	-	200	
t_{CO2}	CE2 Access Time	-	150	-	200	
t_{OE}	Output Enable to Output in Valid	-	70	-	100	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) Output in Low-Z	10	-	10	-	
t_{OEE}	Output Enable to Output Low-Z	5	-	5	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) Output in High-Z	-	70	-	100	
t_{ODO}	Output Enable to Output High-Z	-	60	-	80	
t_{OH}	Output Data Hold Time	20	-	20	-	

WRITE CYCLE

SYMBOL	PARAMETER	TC5564APL-15 TC5564AFL-15		TC5564APL-20 TC5564AFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	150	-	200	-	ns
t_{WP}	Write Pulse Width	100	-	150	-	
t_{CW}	Chip Selection to End of Write	120	-	180	-	
t_{AS}	Address Set Up Time	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	
t_{ODW}	R/W to Output High-Z	-	70	-	100	
t_{OEW}	R/W to Output Low-Z	10	-	10	-	
t_{DS}	Data Set Up Time	60	-	80	-	
t_{DH}	Data Hold Time	0	-	0	-	

AC TEST CONDITION

- Input Pulse Levels : 2.4V/0.6V
- Timing Measurement Reference Levels: 2.2V/0.8V
- Output Reference Levels : 2.2V/0.8V
- Input Pulse Rise and Fall Time : 5ns
- Output Load : See Fig. 1

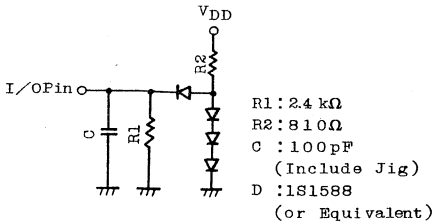
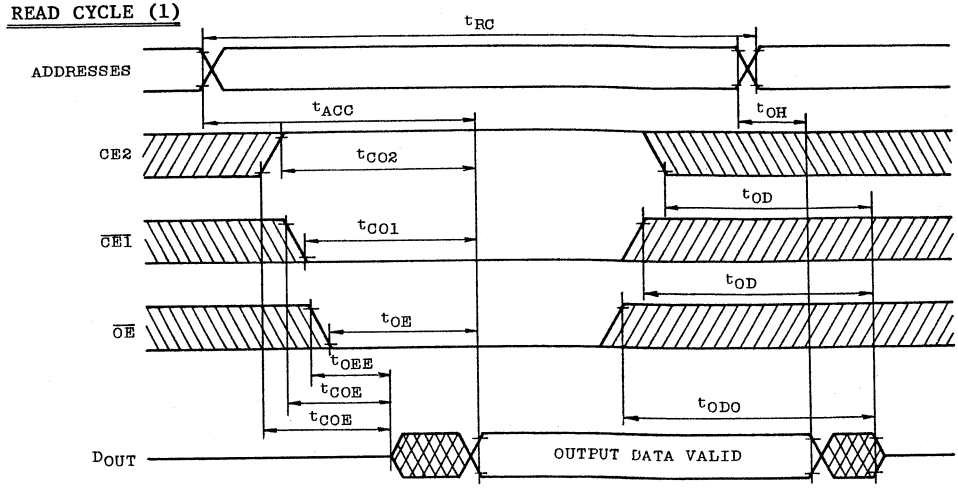


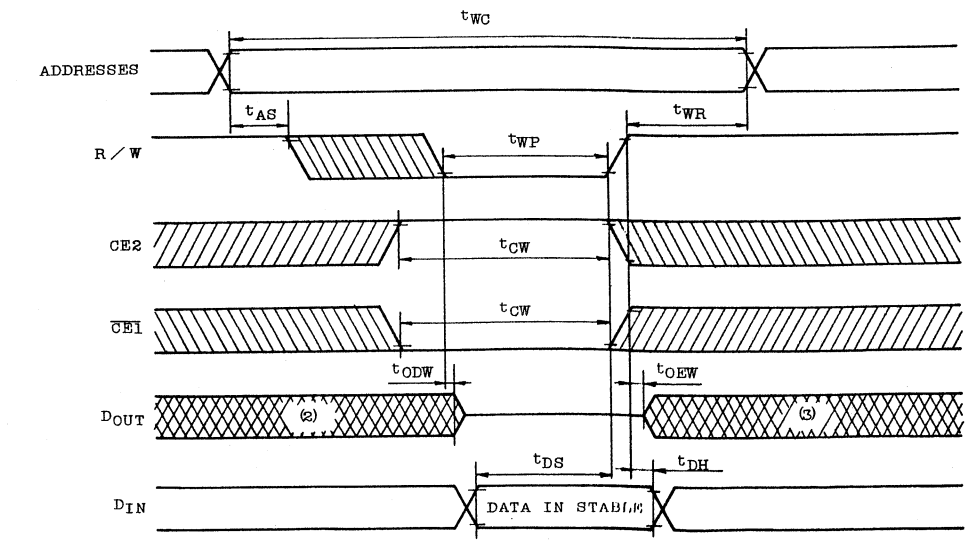
Fig.1 Output load

TIMING WAVEFORMS

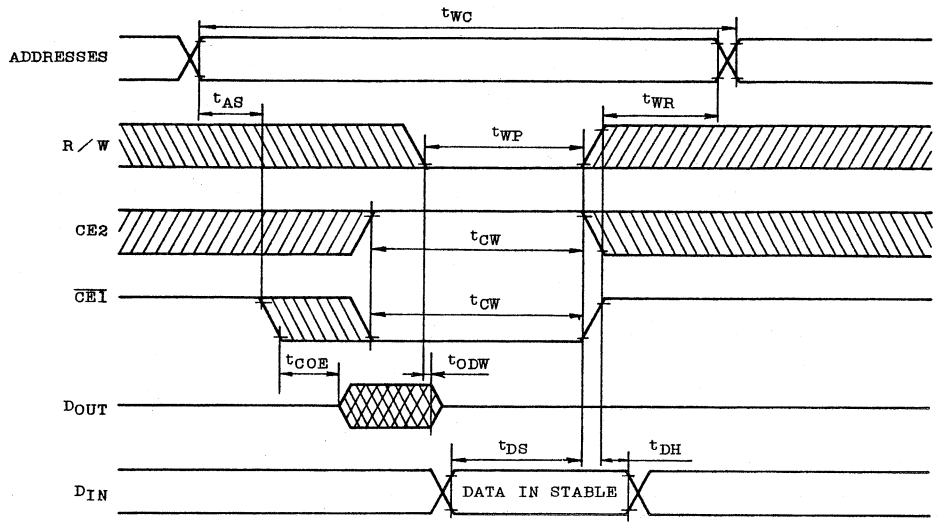
READ CYCLE (1)



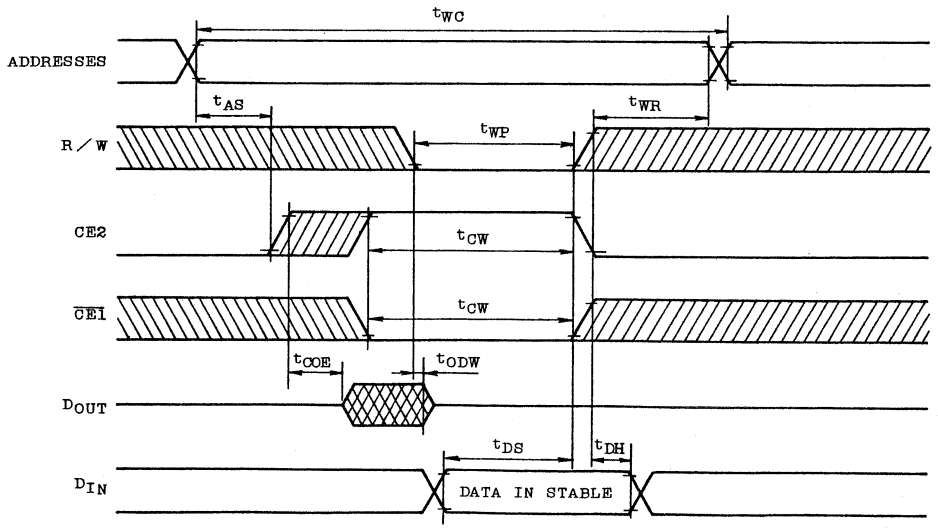
WRITE CYCLE 1 (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



NOTE:

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

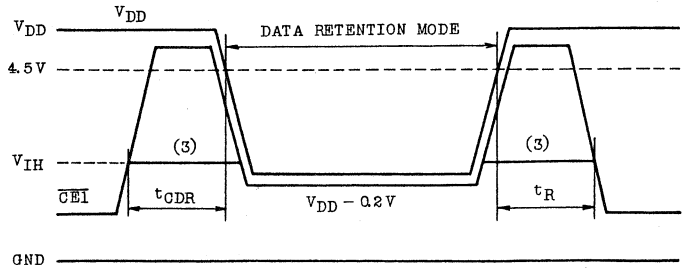
(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

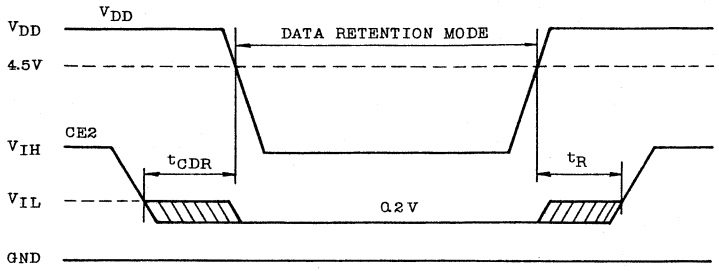
DATA RETENTION CHARACTERISTICS (Ta=-40 ∿ 85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Current	Ta=25°C	-	0.01	0.2	μA
		Ta=60°C	-	-	1.0	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μs
t_R	Recovery Time		t_{RC}(1)	-	-	nS

$\overline{CE1}$ Controlled Data Retention Mode (2)



CE2 Controlled Data Retention Mode (4)



NOTE: (1) t_{RC}: Read Cycle Time

(2) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V or CE2 $\geqq V_{DD}$-0.2V.

(3) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

(4) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V.

DEVICE INFORMATION

The TC5564APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows after only row address change, as is shown in the following figure.

This peak current may induce the noise on V_{DD}/GND line. Thus the use of about 0.1μF decoupling capacitor every device is recommended to eliminate such noise.

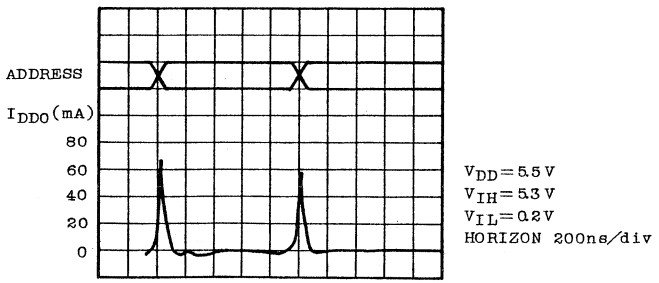


Fig. TYPICAL CURRENT WAVEFORMS

TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

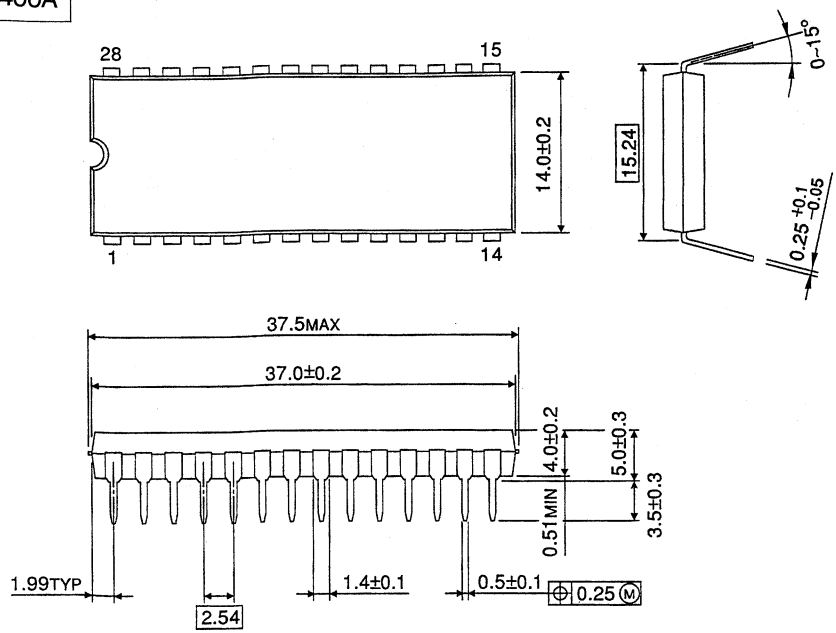
We hope this information will be very useful for you.

Nov. 1991

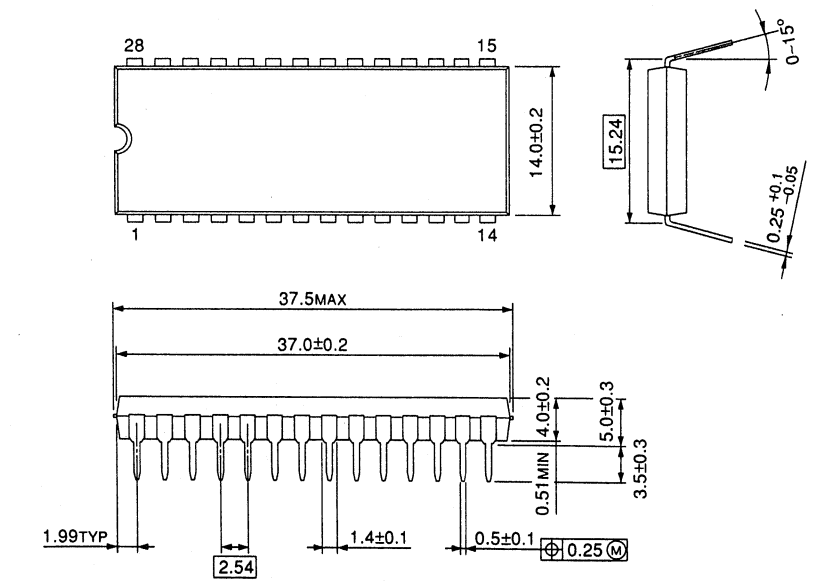
TOSHIBA CORPORATION
Semiconductor Group

Unit in mm

DIP28-P-400A

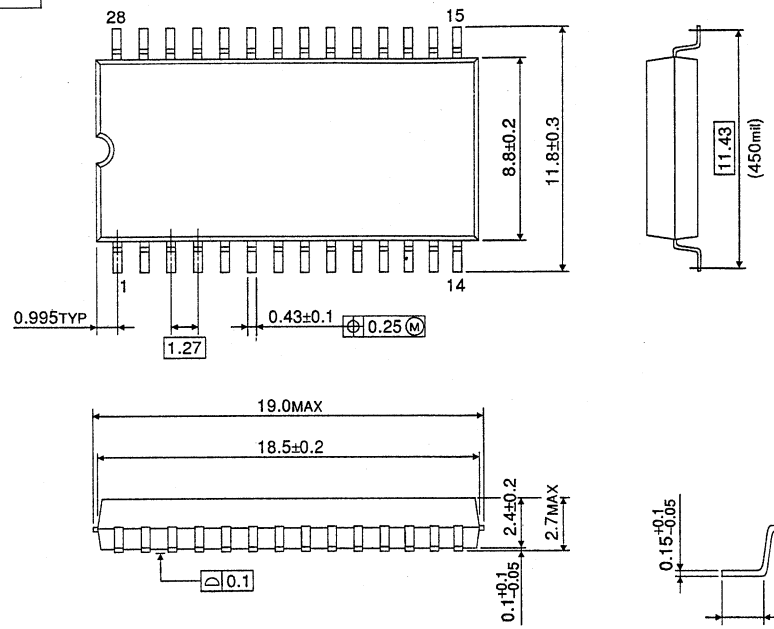


DIP28-P-600



Unit in mm

SOP28-P-450



SOP32-P-450