

TC5588P/J-15,-20,-25,-35

8,192 WORD \times 8 BIT CMOS STATIC RAM

DESCRIPTION

The TC5588P/J is a 65,536 bits high speed static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit from provides high speed feature.

The TC5588P/J has low power feature with device control using Chip Enable ($\overline{CE1}/\overline{CE2}$), and has Output Enable Input (\overline{OE}) for fast memory access. Also the device power at memory access is reduced by automatic power down circuit form.

The TC5588P/J is suitable for use in cache memory where high speed is required, and high speed storage. All Inputs and Outputs are directly TTL compatible.

The TC5588P/J is moulded in 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

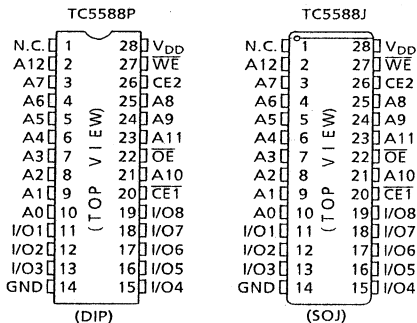
- Fast access time:

TC5588P/J-15	15ns (MAX.)
TC5588P/J-20	20ns (MAX.)
TC5588P/J-25	25ns (MAX.)
TC5588P/J-35	35ns (MAX.)
- Low power dissipation:

Operation	TC5588P/J-15	135mA (MAX.)
	TC5588P/J-20	115mA (MAX.)
	TC5588P/J-25	115mA (MAX.)
	TC5588P/J-35	115mA (MAX.)
Standby		1mA (MAX.)
- 5V single power supply : $5V \pm 10\%$
- Fully static operation
- Directly TTL compatible : All Input and Output
- Output buffer control : \overline{OE}
- Package

TC5588P	: DIP28-P-300B
TC5588J	: SOJ28-P-300A

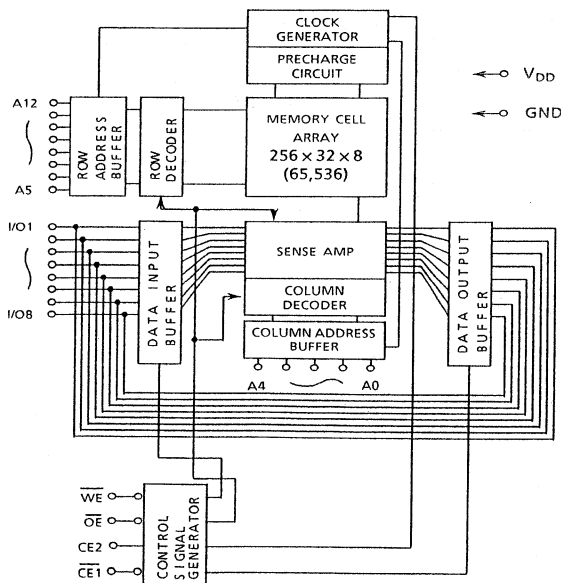
PIN CONNECTION



PIN NAMES

A0~A12	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Inputs
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	$-0.5 \sim 7.0$	V
V_{IN}	Input Voltage	$-2.0 \sim 7.0$	V
V_{OUT}	Output Voltage	$-0.5 \sim V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	$260 \cdot 10$	$^{\circ}\text{C} \cdot \text{sec}$
T_{strg}	Storage Temperature	$-65 \sim 150$	$^{\circ}\text{C}$
T_{opr}	Operating Temperature	$-10 \sim 85$	$^{\circ}\text{C}$

DC RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70^{\circ}\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	* - 3.0	—	0.8	V

* Pulse width $\leq 10\text{ns}$, DC: -0.5V (min)

DC CHARACTERISTICS ($T_a = 0 \sim 70^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	- 4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{DD0}	Operating Current	$V_{DD} = 5.5\text{V}$ tcycle = Min cycle $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ Other Inputs = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$	- 15	—	—	mA
			- 20	—	—	
			- 25	—	—	
			- 35	—	—	
I_{DDS1}	Standby Current	$V_{DD} = 5.5\text{V}$ tcycle = Min cycle $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ Other Inputs = V_{IH}/V_{IL}	—	—	25	mA
I_{DDS2}^*		$\overline{CE1} = V_{DD} - 0.2\text{V}$ or $CE2 = 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	1	

*: In standby mode with $\overline{CE1} \geq V_{DD} - 0.2\text{V}$, these specification limits are guaranteed under the condition of $\overline{CE2} \geq V_{DD} - 0.2\text{V}$ or $CE2 \leq 0.2\text{V}$.

CAPACITANCE ($T_a = 25^{\circ}\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	7	pF

NOTE : This parameter periodically sampled is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C⁽¹⁾, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t _{ACC}	Address Access Time	—	15	—	20	—	25	—	35	
t _{CO1}	CE1 Access Time	—	15	—	20	—	25	—	35	
t _{CO2}	CE2 Access Time	—	15	—	20	—	25	—	35	
t _{OE}	OE Access Time	—	9	—	10	—	12	—	12	
t _{OH}	Output Data Hold Time From Address Change	5	—	5	—	5	—	5	—	
t _{COE}	Output Enable Time from CE1 or CE2	5	—	5	—	5	—	5	—	
t _{COD}	Output Disable Time from CE1 or CE2	—	6	—	6	—	6	—	6	
t _{OEE}	Output Enable Time from OE	0	—	0	—	0	—	0	—	
t _{ODO}	Output Disable Time from OE	—	5	—	5	—	5	—	5	
t _{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	
t _{PD}	Chip Deselection to Power Down Time	—	15	—	20	—	25	—	35	

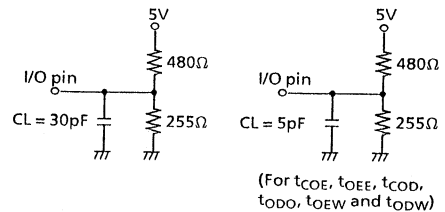
WRITE CYCLE

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	ns
t _{CW}	Chip Enable to End of Write	12	—	13	—	15	—	15	—	
t _{AS}	Address Set Up Time	0	—	0	—	0	—	0	—	
t _{WP}	Write Pulse Width	12	—	13	—	15	—	15	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t _{DS}	Data Set Up Time	9	—	10	—	12	—	12	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t _{OEw}	Output Enable Time from WE	0	—	0	—	0	—	0	—	
t _{ODw}	Output Disable Time from WE	—	6	—	6	—	6	—	6	

AC TEST CONDITIONS

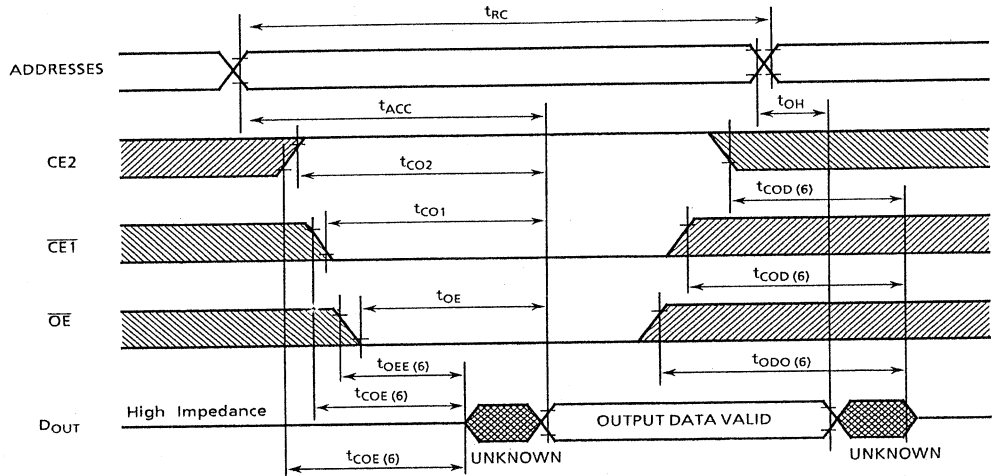
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

Fig. 1

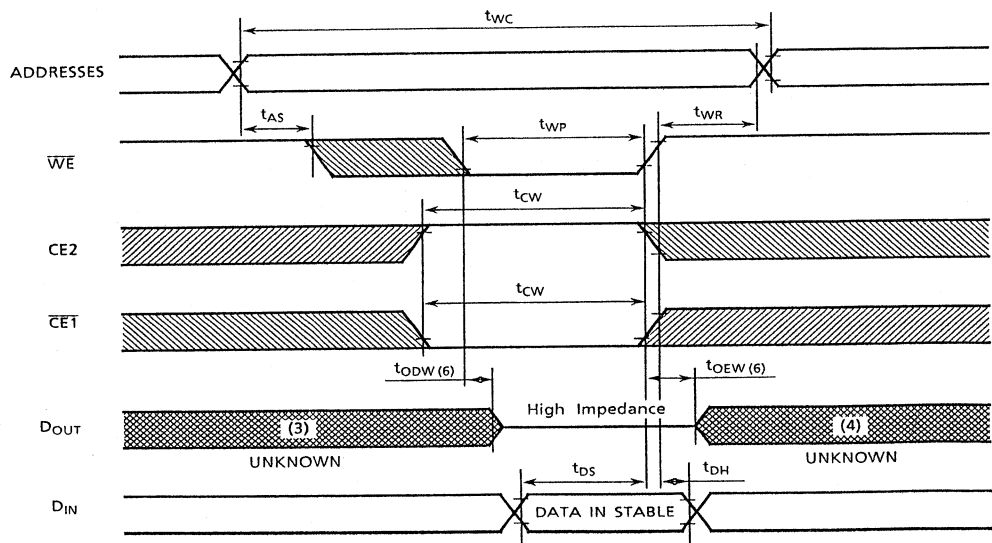


TIMING WAVEFORMS

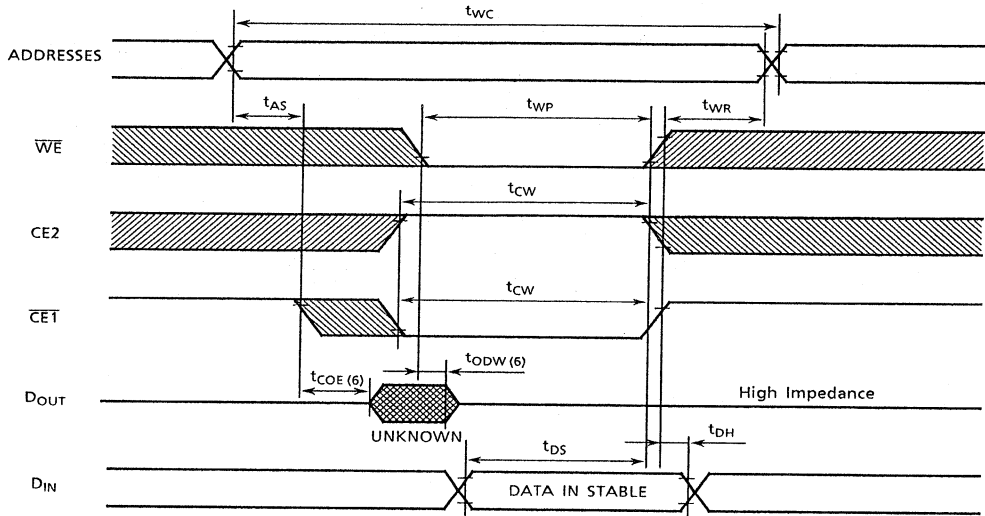
READ CYCLE (2)



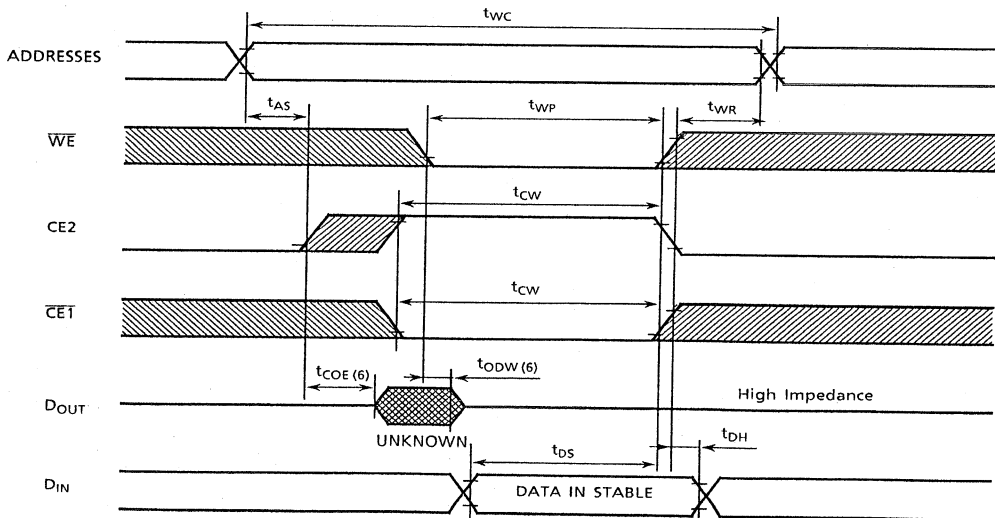
WRITE CYCLE 1 (5) (\overline{WE} Controlled Write)



WRITE CYCLE 2 (5) ($\overline{\text{CE1}}$ Controlled Write)



WRITE CYLCE 3 (5) (CE2 Controlled Write)

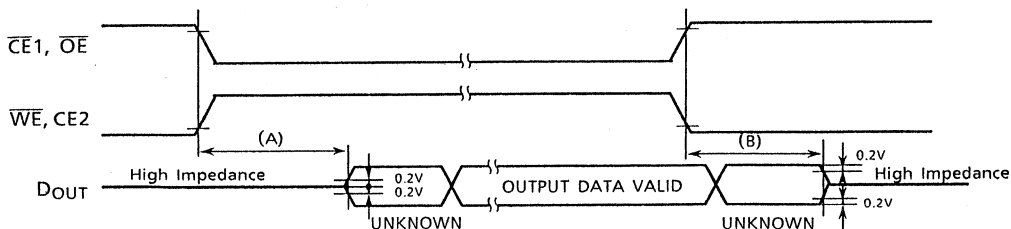


- NOTES: 1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is High for Read Cycle.
3. Assuming that $\overline{CE1}$ Low transition or $CE2$ High transition occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{CE1}$ High transition or $CE2$ Low transition occurs coincident with or prior to \overline{WE} High transition, Outputs remain in a high impedance state.
5. Assuming that \overline{OE} is High for Write Cycle, Outputs are in a high impedance state during this period.
6. These parameters are specified as follows and measured by using the load shown in

Fig. 1.

(A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time

(B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time



TOSHIBA

DATA BOOK

MOS MEMORY (VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

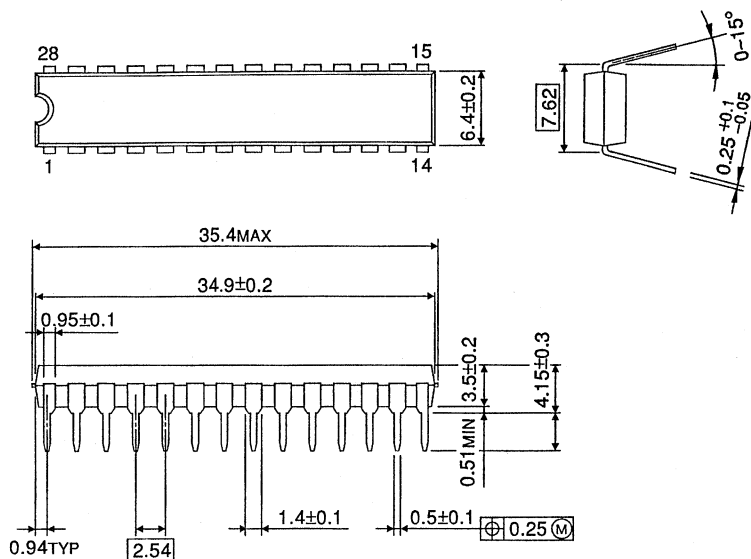
These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

We hope this information will be very useful for you.

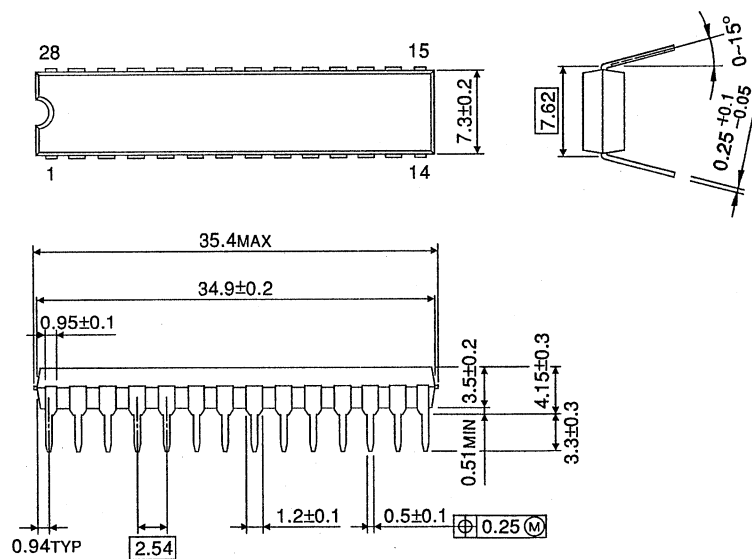
Nov. 1991

TOSHIBA CORPORATION
Semiconductor Group

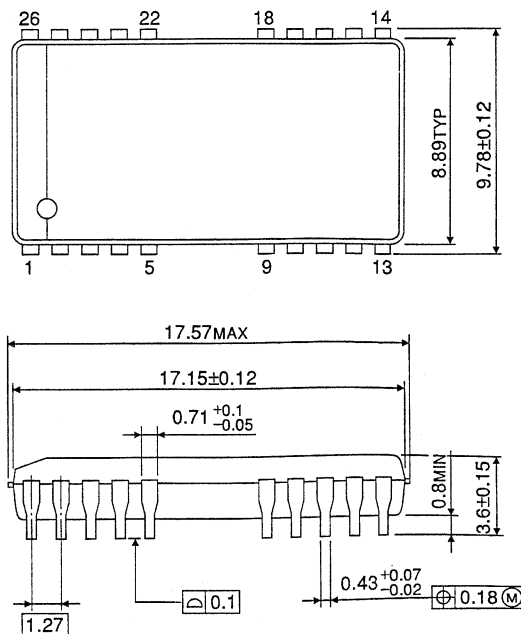
DIP28-P-300A



DIP28-P-300B



SOJ26-P-350



SOJ28-P-300A

