

# TC55B329P/J-10,-12,-15

TENTATIVE DATA

32,768 WORD × 9 BIT BiCMOS STATIC RAM

PRELIMINARY

## DESCRIPTION

The TC55B329P/J is a 294,912 bits high speed static random access memory organized as 32,768 words by 9 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provides high speed feature.

The TC55B329P/J has low power feature with device control using Chip Enable ( $\overline{CE1}/\overline{CE2}$ ), and has Output Enable Input ( $\overline{OE}$ ) for fast memory access.

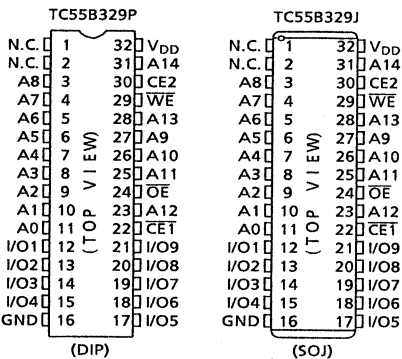
The TC55B329P/J is suitable for use in cache memory where high speed is required, and high speed storage. All Inputs and Outputs are directly TTL compatible.

The TC55B329P/J is moulded in 32 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

## FEATURES

- Fast access time:
  - TC55B329P/J-10      10ns (MAX.)
  - TC55B329P/J-12      12ns (MAX.)
  - TC55B329P/J-15      15ns (MAX.)
- Low power dissipation
  - Operation : TC55B329P/J-10    170mA (MAX.)
  - TC55B329P/J-12    170mA (MAX.)
  - TC55B329P/J-15    170mA (MAX.)
  - Standby :                            15mA (MAX.)
- 5V single power supply : 5V ± 10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control :  $\overline{OE}$
- Package
  - TC55B329P : DIP32-P-300
  - TC55B329J : SOJ32-P-300

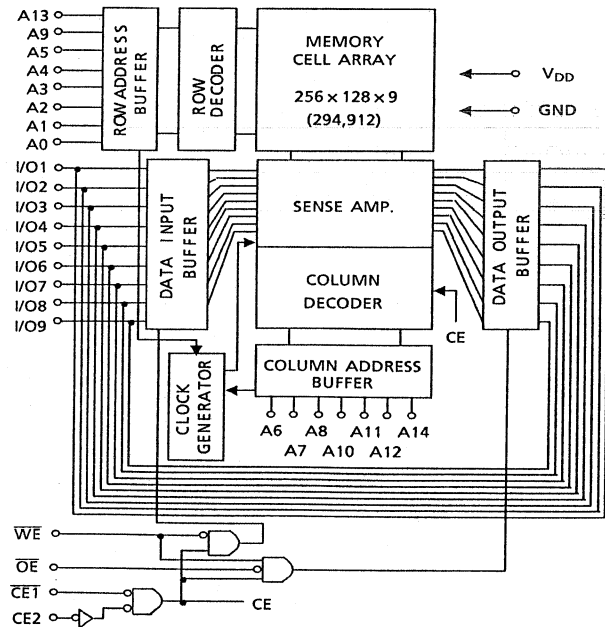
## PIN CONNECTION



## PIN NAMES

A0~A14	Address Inputs
I/O1~I/O9	Data Inputs/Outputs
$\overline{CE1}$ , CE2	Chip Enable Inputs
WE	Write Enable Input
$\overline{OE}$	Output Enable Input
V <sub>DD</sub>	Power (+5V)
GND	Ground
N.C.	No Connection

## BLOCK DIAGRAM



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## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.5~7.0	V
V <sub>IN</sub>	Input Voltage	-2.0~7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-0.5*~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.0	W
T <sub>solder</sub>	Soldering Temperature · Time	260 · 10	°C · sec
T <sub>strg</sub>	Storage Temperature	-65~150	°C
T <sub>opr</sub>	Operating Temperature	-10~85	°C

\* : -3V with a pulse width of 10ns

## DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5*	-	0.8	V

\* : -3V with a pulse width of 10ns

## DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V<sub>DD</sub> = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0~V <sub>DD</sub>	-	-	±10	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>OUT</sub> = 0~V <sub>DD</sub>	-	-	±10	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-4	-	-	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	8	-	-	mA
I <sub>DDO</sub>	Operating Current	t <sub>cycle</sub> = Min cycle, $\overline{CE1} = V_{IL}$ and CE2 = V <sub>IH</sub> Other Inputs = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>out</sub> = 0mA	-	-	170	mA
I <sub>DDs1</sub>	Standby Current	$\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub> Other Inputs = V <sub>IH</sub> or V <sub>IL</sub>	-	-	30	mA
I <sub>DDs2</sub>		$\overline{CE1} = V_{DD} - 0.2V$ or CE2 = 0.2V Other Inputs = V <sub>DD</sub> - 0.2V or 0.2V	-	-	15	

**CAPACITANCE** (Ta = 25°C, f = 1.0MHZ)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	6	pF
C <sub>I/O</sub>	Input / Output Capacitance	V <sub>I/O</sub> = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

**OPERATING MODE**

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O1~I/O9	POWER
Read	L	H	L	H	Output	I <sub>DDO</sub>
Write	L	H	*	L	Input	I <sub>DDO</sub>
Output Disable	L	H	H	H	High Impedance	I <sub>DDO</sub>
Standby	H	*	*	*	High Impedance	I <sub>DDS</sub>
	*	L	*	*	High Impedance	I <sub>DDS</sub>

\* : H or L

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## AC CHARACTERISTICS (Ta = 0~70°C <sup>(1)</sup>, V<sub>DD</sub> = 5V ± 10%)

### READ CYCLE

SYMBOL	PARAMETER	TC55B329P/J - 10		TC55B329P/J - 12		TC55B329P/J - 15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	10	-	12	-	15	-	ns
t <sub>ACC</sub>	Address Access Time	-	10	-	12	-	15	
t <sub>CO1</sub>	$\overline{CE1}$ Access Time	-	10	-	12	-	15	
t <sub>CO2</sub>	CE2 Access Time	-	10	-	12	-	15	
t <sub>OE</sub>	$\overline{OE}$ Access Time	-	5	-	6	-	8	
t <sub>OH</sub>	Output Data Hold Time from Address Change	3	-	3	-	3	-	
t <sub>COE</sub>	Output Enable Time from $\overline{CE1}$ or CE2	3	-	3	-	3	-	
t <sub>COD</sub>	Output Disable Time from $\overline{CE1}$ or CE2	-	5	-	6	-	6	
t <sub>OEE</sub>	Output Enable Time from $\overline{OE}$	1	-	1	-	1	-	
t <sub>ODO</sub>	Output Disable Time from $\overline{OE}$	-	5	-	6	-	6	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	-	0	-	0	-	
t <sub>PD</sub>	Chip Deselection to Power Down Time	-	10	-	12	-	15	

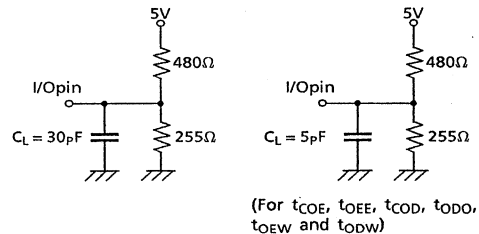
### WRITE CYCLE

SYMBOL	PARAMETER	TC55B329P/J - 10		TC55B329P/J - 12		TC55B329P/J - 15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	10	-	12	-	15	-	ns
t <sub>CW</sub>	Chip Enable to End of Write	7	-	8	-	9	-	
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	0	-	
t <sub>AW</sub>	Address valid to end of write	7	-	8	-	9	-	
t <sub>WP</sub>	Write Pulse Width	6	-	7	-	8	-	
t <sub>WR</sub>	Write Recovery Time	1	-	1	-	1	-	
t <sub>DS</sub>	Data Set Up Time	6	-	7	-	8	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	
t <sub>OE<sub>W</sub></sub>	Output Enable Time from $\overline{WE}$	1	-	1	-	1	-	
t <sub>OD<sub>W</sub></sub>	Output Disable Time from $\overline{WE}$	-	5	-	6	-	6	

### AC TEST CONDITIONS

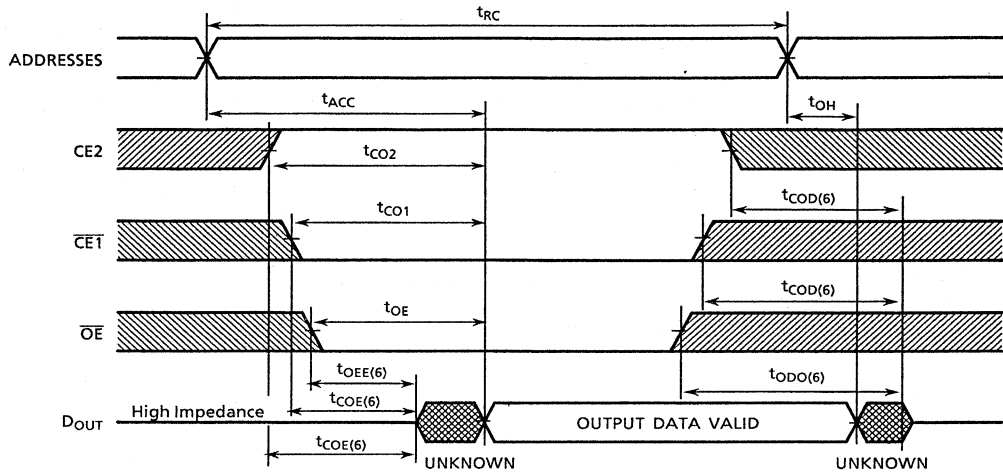
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig.1

Fig.1

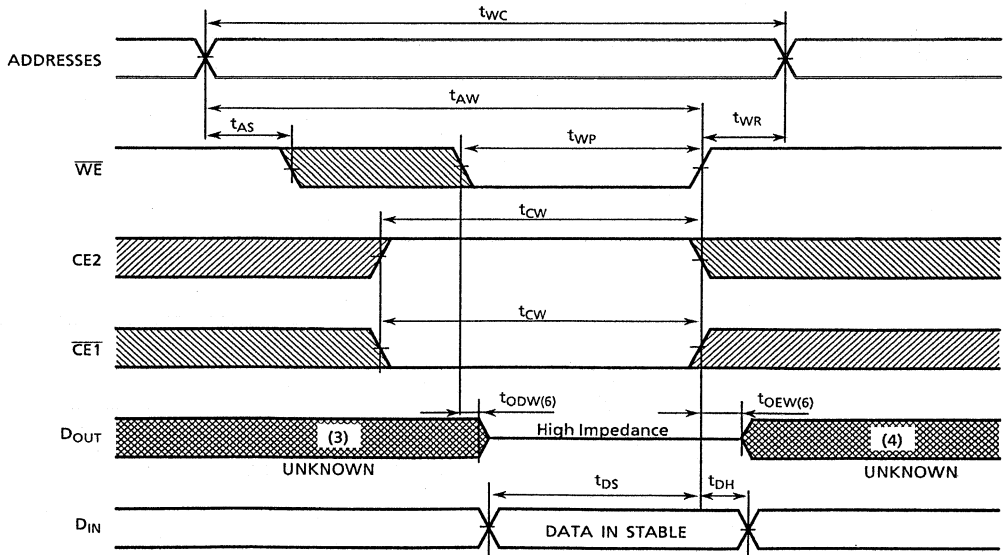


**TIMING WAVEFORMS**

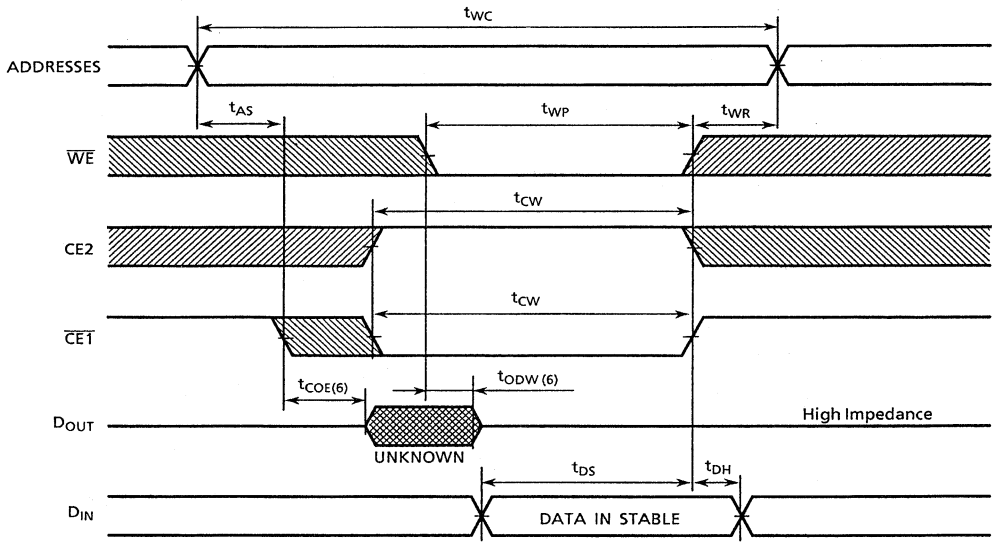
**READ CYCLE (2)**



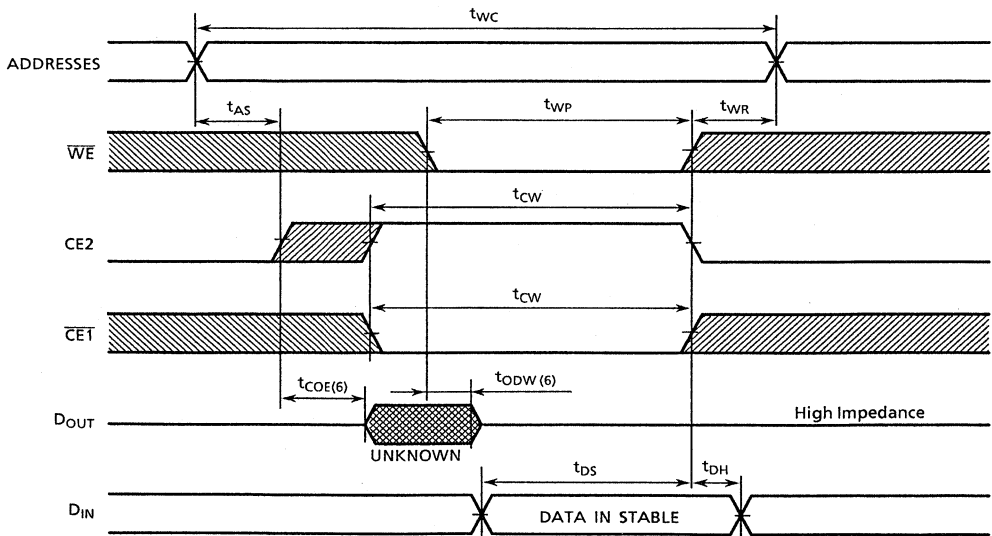
**WRITE CYCLE1 (5) ( $\overline{WE}$  Controlled Write)**



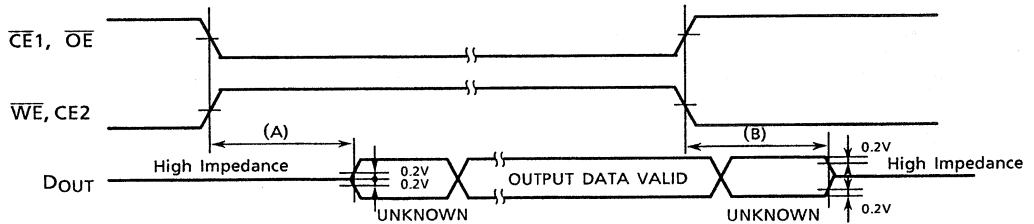
WRITE CYCLE 2 (5) ( $\overline{CE1}$  Controlled Write)



WRITE CYCLE 3 (5) (CE2 Controlled Write)



- NOTE: 1. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2.  $\overline{WE}$  is High for Read Cycle.
  3. Assuming that  $\overline{CE1}$  Low transition or CE2 High transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
  4. Assuming that  $\overline{CE1}$  High transition or CE2 Low transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
  5. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in a high impedance state during this period.
  6. These parameters are specified as follows and measured by using the load shown in Fig.1.
    - (A)  $t_{COE}$ ,  $t_{OEE}$ ,  $t_{OE\overline{W}}$  ..... Output Enable Time
    - (B)  $t_{COD}$ ,  $t_{ODO}$ ,  $t_{OD\overline{W}}$  ..... Output Disable Time



**TOSHIBA**

DATA BOOK

**MOS MEMORY**  
(VRAM, SRAM)

**1991**



# INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

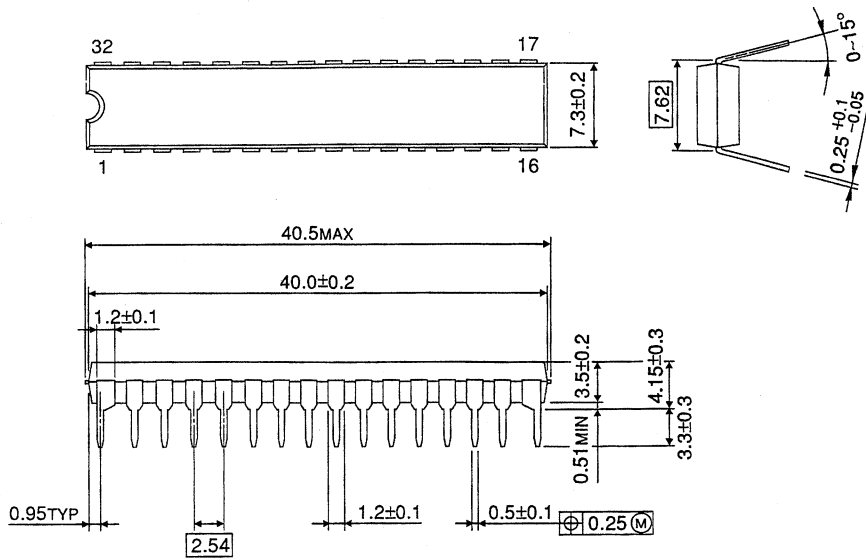
These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

We hope this information will be very useful for you.

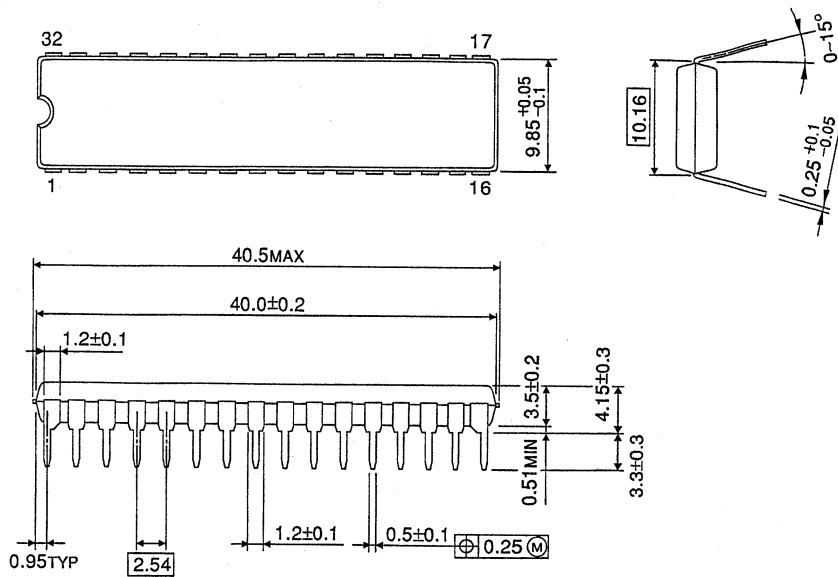
Nov. 1991

TOSHIBA CORPORATION  
Semiconductor Group

DIP32-P-300

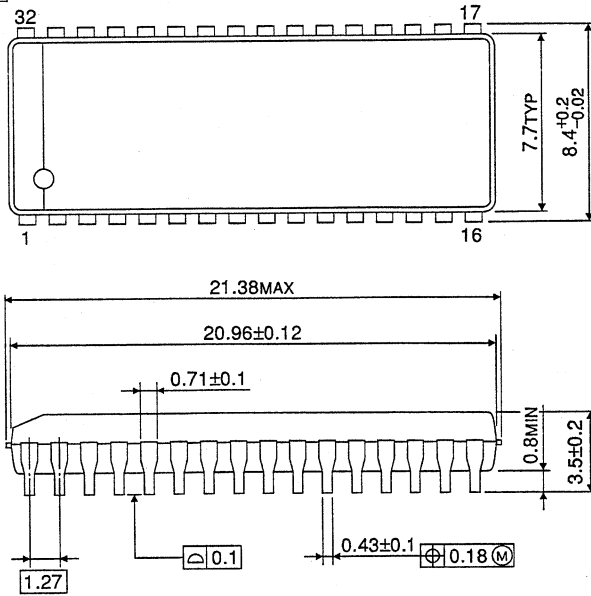


DIP32-P-400



Unit in mm

SOJ32-P-300



SOJ32-P-400

