TC55B464P/J-10,-12,-15

TENTATIVE DATA

65,536 WORD × 4 BIT BiCMOS STATIC RAM

PRELIMINARY

DESCRIPTION

The TC55B464P/J is a 262,144 bits high speed static random access memory organized as 65,536 words by 4 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provides high speed feature.

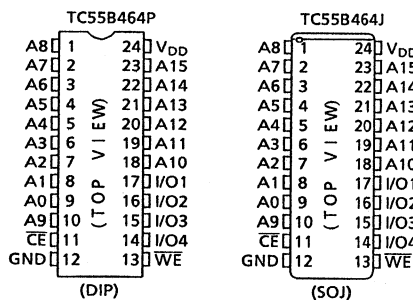The TC55B464P/J has low power feature with device control using Chip Enable ($\overline{CE}$).

The TC55B464P/J is suitable for use in cache memory where high speed is required, and high speed storage. All Inputs and Outputs are directly TTL compatible.

The TC55B464P/J is moulded in 24 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- Fast access time :

TC55B464P/J-10	10ns(MAX.)
TC55B464P/J-12	12ns(MAX.)
TC55B464P/J-15	15ns(MAX.)

- Low power dissipation

  Operation :
TC55B464P/J-10	140mA(MAX.)
TC55B464P/J-12	140mA(MAX.)
TC55B464P/J-15	140mA(MAX.)

  Standby : 15mA(MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Package
 - TC55B464P : DIP24-P-300B
  - TC55B464J : SOJ24-P-300A

PIN CONNECTION

TC55B464P

A8	1	24	V_DD
A7	2	23	A15
A6	3	22	A14
A5	4	21	A13
A4	5	20	A12
A3	6	19	A11
A2	7	18	A10
A1	8	17	I/O1
A0	9	16	I/O2
A9	10	15	I/O3
$\overline{CE}$	11	14	I/O4
GND	12	13	$\overline{WE}$

(TOP VIEW) (DIP)

TC55B464J

A8	1	24	V_DD
A7	2	23	A15
A6	3	22	A14
A5	4	21	A13
A4	5	20	A12
A3	6	19	A11
A2	7	18	A10
A1	8	17	I/O1
A0	9	16	I/O2
A9	10	15	I/O3
$\overline{CE}$	11	14	I/O4
GND	12	13	$\overline{WE}$

(TOP VIEW) (SOJ)

PIN NAMES

A0~A15	Address Inputs
I/O1~I/O4	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_DD	Power(+ 5V)
GND	Ground

BLOCK DIAGRAM

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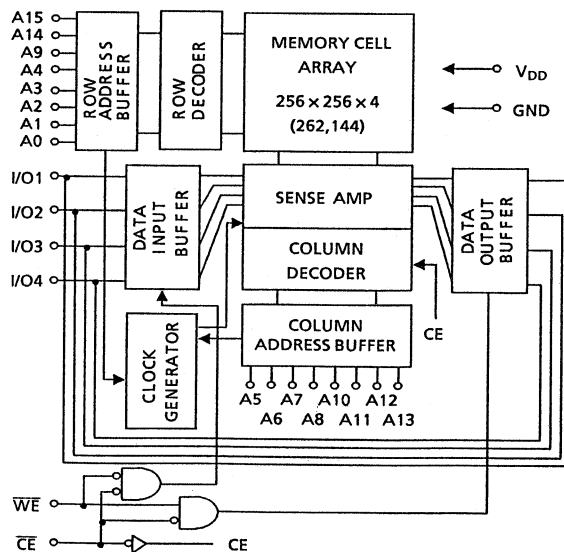
MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	$-0.5 \sim 7.0$	V
V_{IN}	Input Voltage	$-2.0 \sim 7.0$	V
$V_{I/O}$	Input/Output Voltage	$-0.5^* \sim V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	$-65 \sim 150$	°C
T_{opr}	Operating Temperature	$-10 \sim 85$	°C

∗ : −3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5^*	–	0.8	V

∗ : −3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	–	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	–	–	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	–	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	–	–	mA
I_{DDO}	Operating Current	tcycle = Min cycle $\overline{CE} = V_{IL}$ Other Inputs = V_{IH}/V_{IL}, $I_{OUT} = 0mA$	–	–	140	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$ Other Inputs = V_{IH} or V_{IL}	–	–	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	–	–	15	

<u>CAPACITANCE</u> (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

OPERATION MODE	$\overline{CE}$	$\overline{WE}$	I/O1~I/O4	POWER
Read	L	H	Output	I_{DDO}
Write	L	L	Input	I_{DDO}
Standby	H	*	High Impedance	I_{DDS}

* : H or L

AC CHARACTERISTICS (Ta = 0~70°C (1), V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B464P/J-10		TC55B464P/J-12		TC55B464P/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	–	12	–	15	–	ns
t_{ACC}	Address Access Time	–	10	–	12	–	15	ns
t_{CO}	$\overline{CE}$ Access Time	–	10	–	12	–	15	ns
t_{OH}	Output Data Hold Time from Address Change	3	–	3	–	3	–	ns
t_{COE}	Output Enable Time from $\overline{CE}$	3	–	3	–	3	–	ns
t_{COD}	Output Disable Time from $\overline{CE}$	–	5	–	6	–	6	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	10	–	12	–	15	ns

WRITE CYCLE

SYMBOL	PARAMETER	TC55B464P/J-10		TC55B464P/J-12		TC55B464P/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	–	12	–	15	–	ns
t_{CW}	Chip Enable to End of Write	7	–	8	–	9	–	ns
t_{AS}	Address Set Up Time	0	–	0	–	0	–	ns
t_{AW}	Address Valid to end of write	7	–	8	–	9	–	ns
t_{WP}	Write Pulse Width	6	–	7	–	8	–	ns
t_{WR}	Write Recovery Time	1	–	1	–	1	–	ns
t_{DS}	Data Set Up Time	6	–	7	–	8	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	ns
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	ns
t_{ODW}	Output Disable Time from $\overline{WE}$	–	5	–	6	–	6	ns

AC TEST CONDITIONS

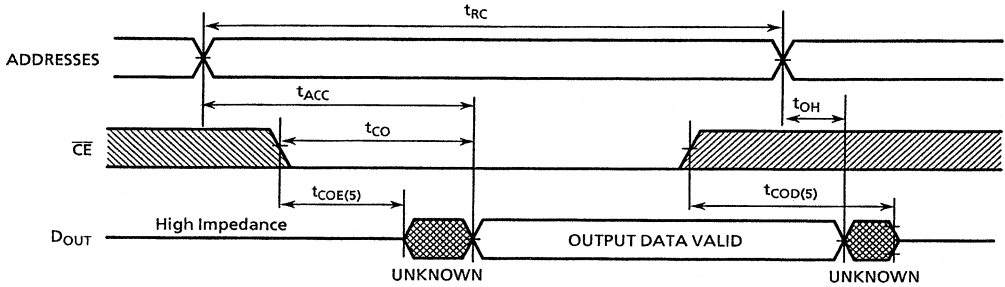|	
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Ref – erence Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

Fig. 1

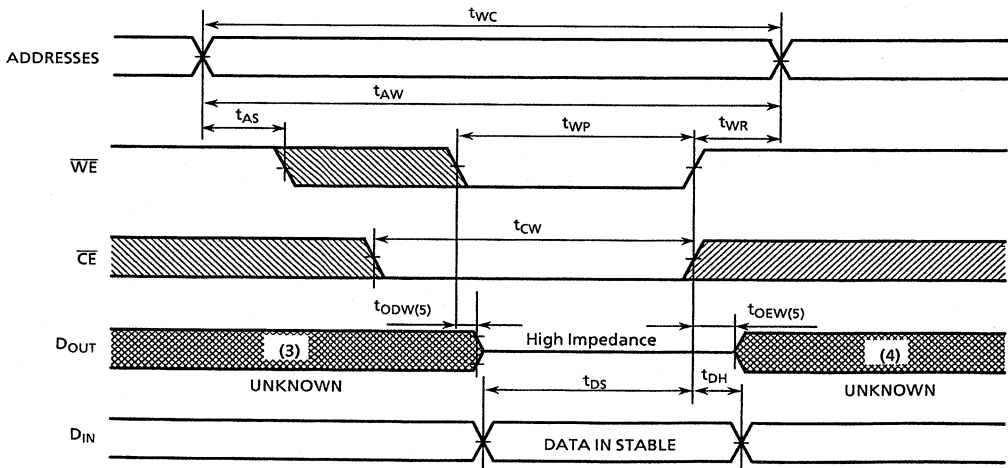

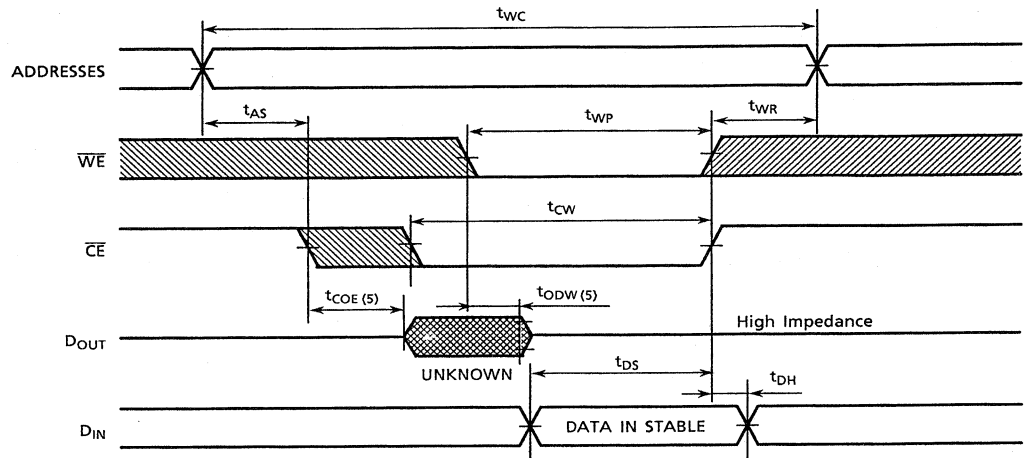(For t_{COE}, t_{COD}, t_{OEW} and t_{ODW})
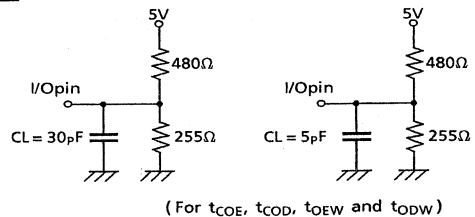
TIMING WAVEFORMS

READ CYCLE (2)

WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)

WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

Note : 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear

feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{COE}, t_{OEW} ⋯⋯ Output Enable Time

(B) t_{COD}, t_{ODW} ⋯⋯ Output Disable Time
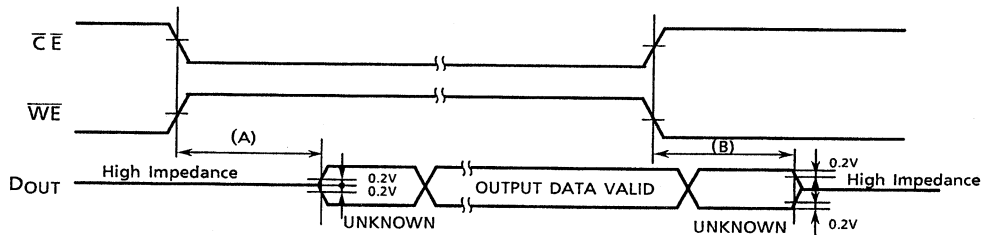
TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that
we may develop and offer to you a diverse array of semicon-
ductor memory products which may be used in many commercial
and industrial applications. At this time, we offer three data books;
"MOS-Memory Dynamic RAM and Module", "MOS-Memory
Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and
Static RAM" edition.

These data books represent our current culminations of electrical
characteristics, timing waveforms and package data for our line
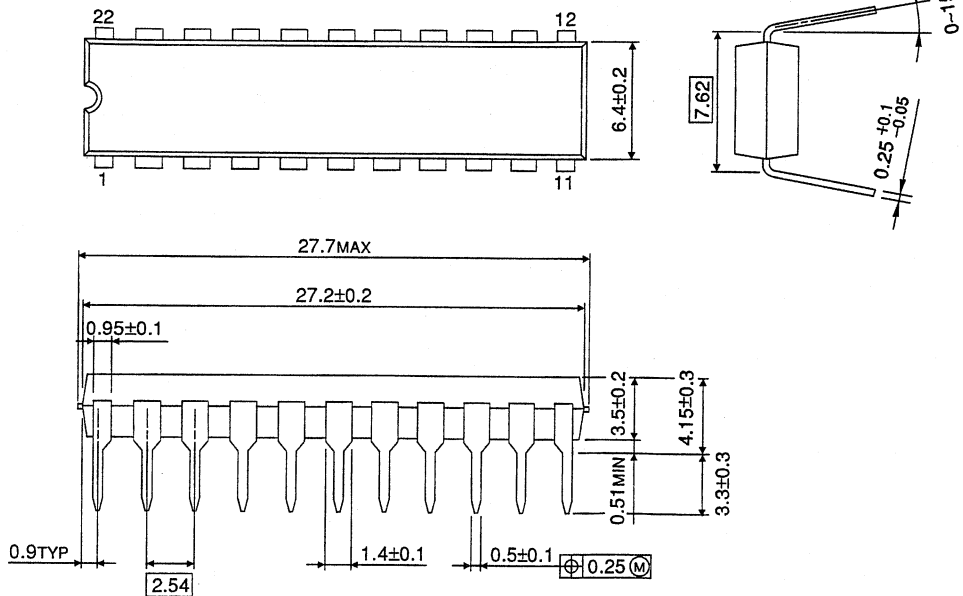of semiconductor memory products.

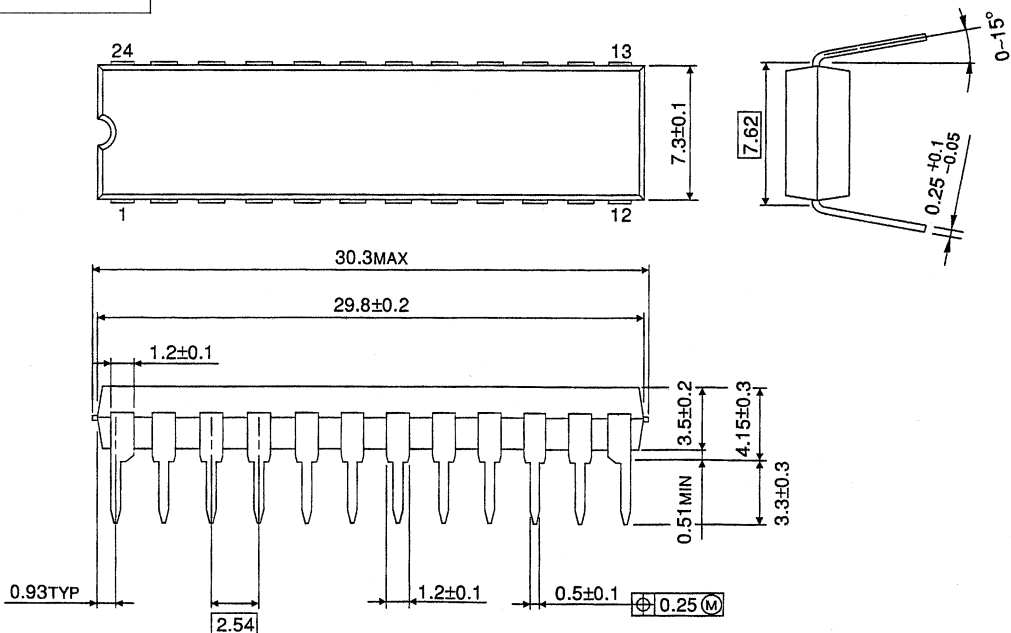We hope this information will be very useful for you.
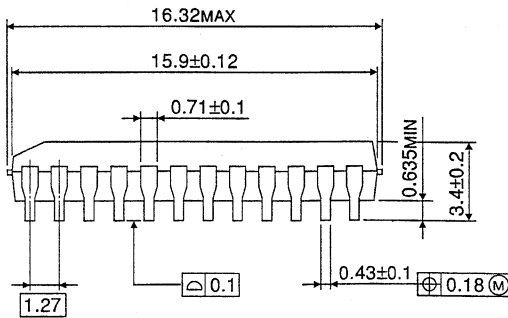
Nov. 1991

TOSHIBA CORPORATION
Semiconductor Group

DIP22-P-300

22   12

1   11

6.4±0.2

7.62

0~15°

0.25 +0.1 −0.05

27.7MAX

27.2±0.2

0.95±0.1

3.5±0.2

4.15±0.3

0.51MIN

3.3±0.3

0.9TYP

1.4±0.1

0.5±0.1

0.25 Ⓜ

2.54

DIP24-P-300B

24   13

1   12

7.3±0.1

7.62

0~15°

0.25 +0.1 −0.05

30.3MAX

29.8±0.2

1.2±0.1

3.5±0.2

4.15±0.3

0.51MIN

3.3±0.3

0.93TYP

1.2±0.1

0.5±0.1

0.25 Ⓜ

2.54

SOJ24-P-300

16.32MAX
15.9±0.12
0.71±0.1
0.635MIN
3.4±0.2
1.27
0.43±0.1
0.18 Ⓜ
7.7TYP
8.4 +0.2 −0.02
6.8TYP
0.2 +0.1 −0.05

SOJ24-P-300A

16.3MAX
15.88±0.12
0.71 +0.1 −0.05
0.8MIN
3.5±0.2
1.27
0.43 +0.07 −0.02
0.18 Ⓜ
7.7TYP
8.4 +0.2 −0.02
6.8TYP
0.2 +0.1 −0.05