SILICON GATE BiCMOS DIGITAL INTEGRATED CIRCUIT

TC55B465P/J-10,-12,-15

TENTATIVE DATA

65,536 WORD × 4 BIT BiCMOS STATIC RAM

PRELIMINART

DESCRIPTION

The TC55B465P/J is a 262,144 bits high speed static random access memory organized as 65,536 words by 4 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provides high speed feature.

The TC55B465P/J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access.

The TC55B465P/J is suitable for use in cache memory where high speed is required, and high speed storage. All Inputs and Outputs are directly TTL compatible.

The TC55B465P/J is moulded in 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- Fast access time :

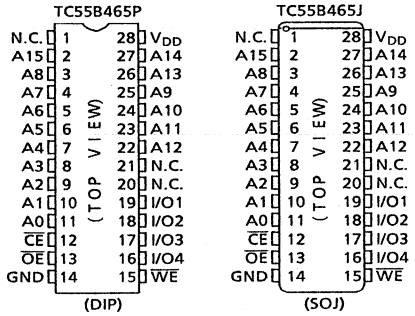
TC55B465P/J−10	10ns (MAX.)
TC55B465P/J−12	12ns (MAX.)
TC55B465P/J−15	15ns (MAX.)

- Low power dissipation

Operation :	TC55B465P/J−10	140mA (MAX.)
	TC55B465P/J−12	140mA (MAX.)
	TC55B465P/J−15	140mA (MAX.)
Standby :		15mA (MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package
  - TC55B465P : DIP28−P−300B
  - TC55B465J : SOJ28−P−300A

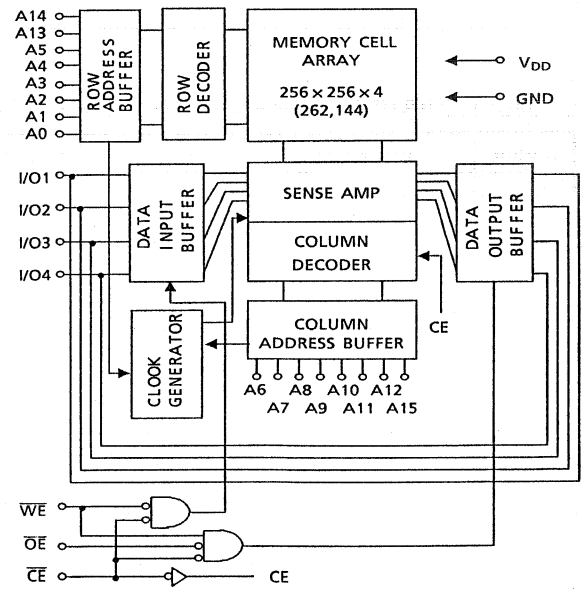
PIN CONNECTION



PIN NAMES

A0~A15	Address Inputs
I/01~I/04	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

*: −3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	−0.5*	−	0.8	V

*: −3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	−	−	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}	−	−	± 10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	−	−	mA
I_{DDO}	Operating Current	tcycle = Min cycle, $\overline{CE}$ = V_{IL} Other Inputs = V_{IH}/V_{IL}, I_{OUT} = 0mA	−	−	140	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH} or V_{IL}	−	−	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Inputs = V_{DD} − 0.2V or 0.2V	−	−	15	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O1~I/O4	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Output Disable	L	H	H	High Impedance	I_{DDO}
Standby	H	*	*	High Impedance	I_{DDS}

* : H or L

AC CHARACTERISTICS (Ta = 0~70°C(1) 、 V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B465P/J-10		TC55B465P/J-12		TC55B465P/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	–	12	–	15	–	ns
t_{ACC}	Address Access Time	–	10	–	12	–	15	ns
t_{CO}	$\overline{CE}$ Access Time	–	10	–	12	–	15	ns
t_{OE}	$\overline{OE}$ Access Time	–	5	–	6	–	8	ns
t_{OH}	Output Data Hold Time from Address Change	3	–	3	–	3	–	ns
t_{COE}	Output Enable Time from $\overline{CE}$	3	–	3	–	3	–	ns
t_{COD}	Output Disable Time from $\overline{CE}$	–	5	–	6	–	6	ns
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	1	–	ns
t_{ODO}	Output Disable Time from $\overline{OE}$	–	5	–	6	–	6	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	10	–	12	–	15	ns

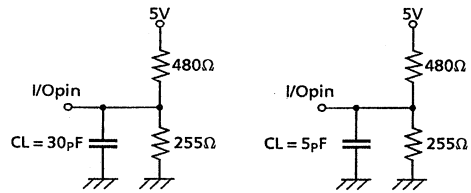
WRITE CYCLE

SYMBOL	PARAMETER	TC55B465P/J-10		TC55B465P/J-12		TC55B465P/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	–	12	–	15	–	ns
t_{CW}	Chip Enable to End of Write	7	–	8	–	9	–	ns
t_{AS}	Address Set Up Time	0	–	0	–	0	–	ns
t_{AW}	Address Valid to end of write	7	–	8	–	9	–	ns
t_{WP}	Write Pulse Width	6	–	7	–	8	–	ns
t_{WR}	Write Recovery Time	1	–	1	–	1	–	ns
t_{DS}	Data Set Up Time	6	–	7	–	8	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	ns
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	ns
t_{ODW}	Output Disable Time from $\overline{WE}$	–	5	–	6	–	6	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Ref – erence Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

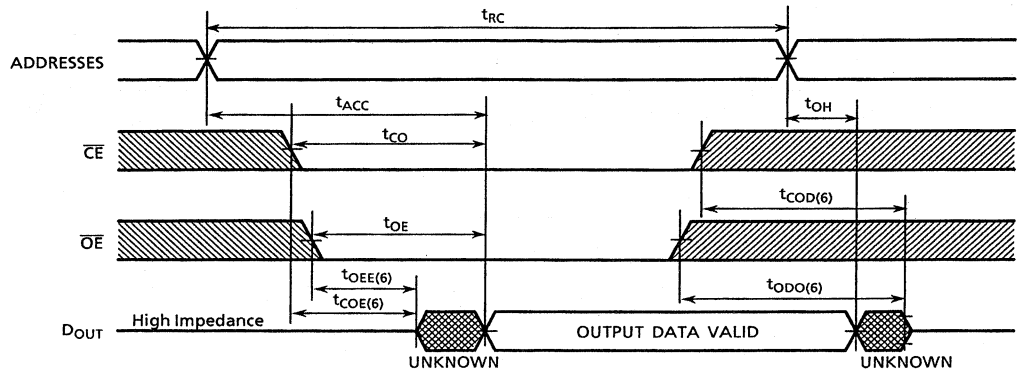
Fig. 1



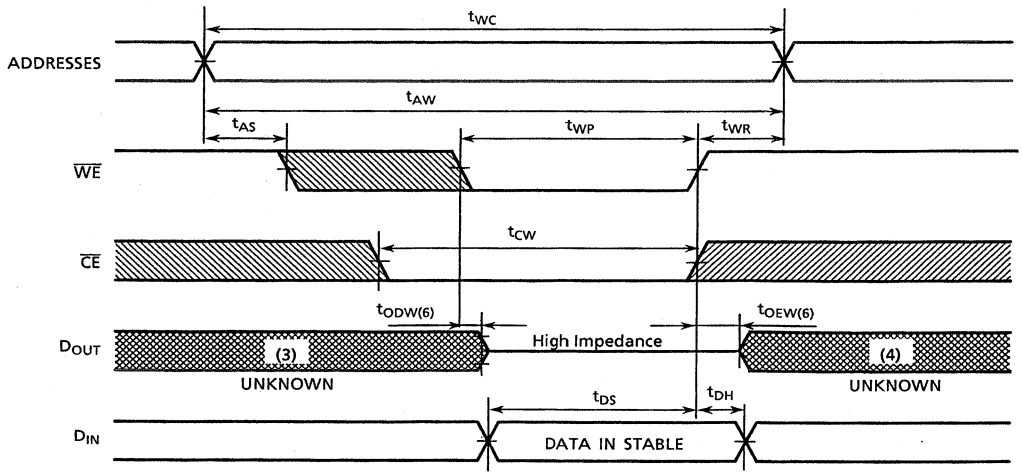
(For t_{COE}, t_{OEE}, t_{COD}, t_{ODO}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

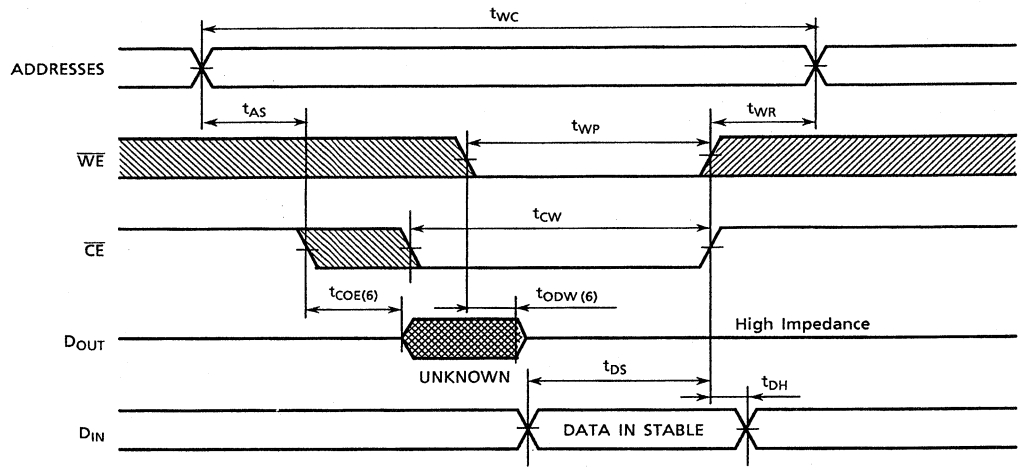
READ CYCLE (2)



WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE2 (5) ($\overline{CE}$ Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

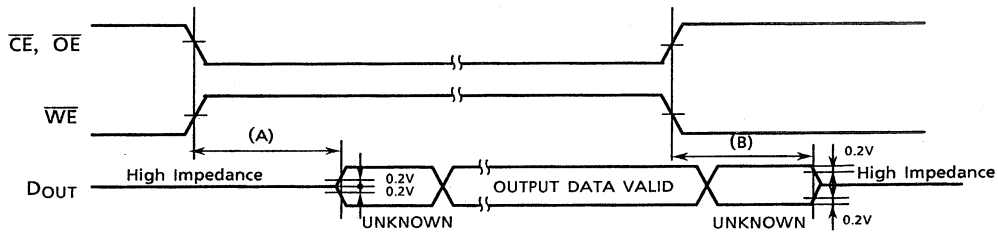
4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ····· Output Enable Time

   (B) t_{COD}, t_{ODO}, t_{ODW} ····· Output Disable Time



TOSHIBA

DATA BOOK

MOS MEMORY

(VRAM, SRAM)

1991

INTRODUCTION

We continually venture at the leading edge of technology so that we may develop and offer to you a diverse array of semiconductor memory products which may be used in many commercial and industrial applications. At this time, we offer three data books; "MOS-Memory Dynamic RAM and Module", "MOS-Memory Video RAM and Static RAM" and "MOS-Memory ROM".

Particularly, this data book is "MOS-Memory Video RAM and Static RAM" edition.

These data books represent our current culminations of electrical characteristics, timing waveforms and package data for our line of semiconductor memory products.

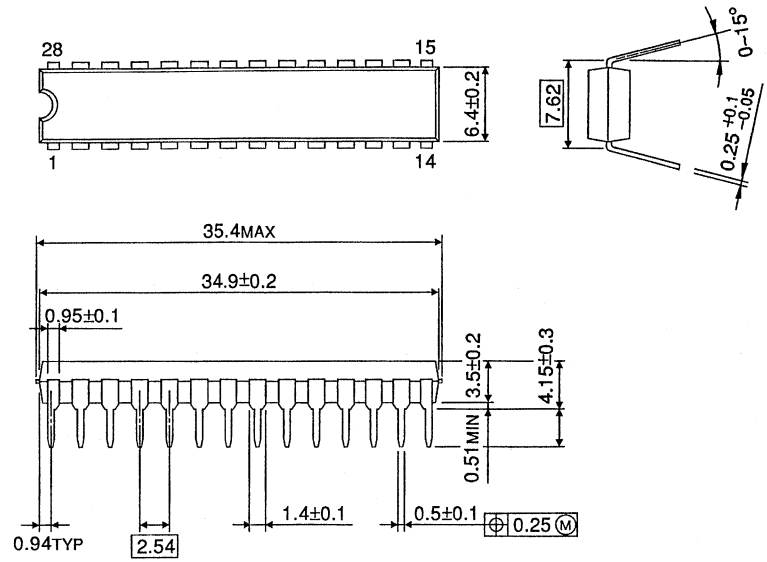
We hope this information will be very useful for you.

Nov. 1991

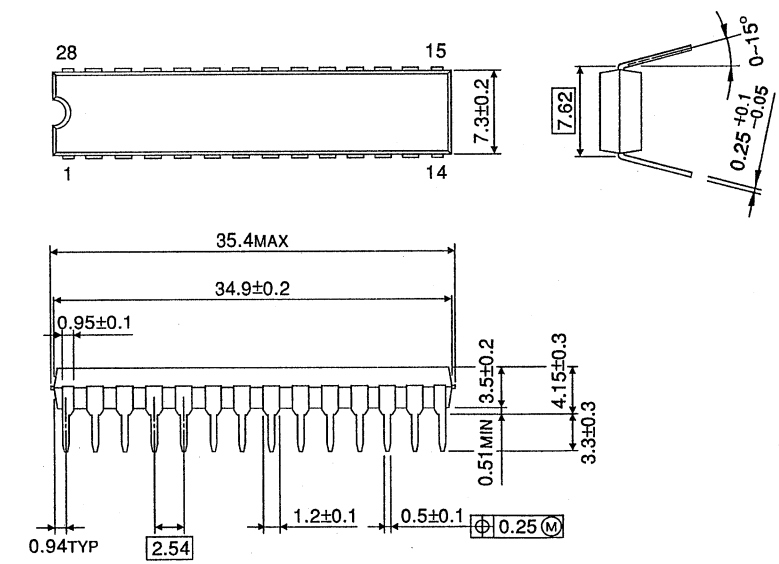
TOSHIBA CORPORATION
Semiconductor Group

Unit in mm

DIP28-P-300A

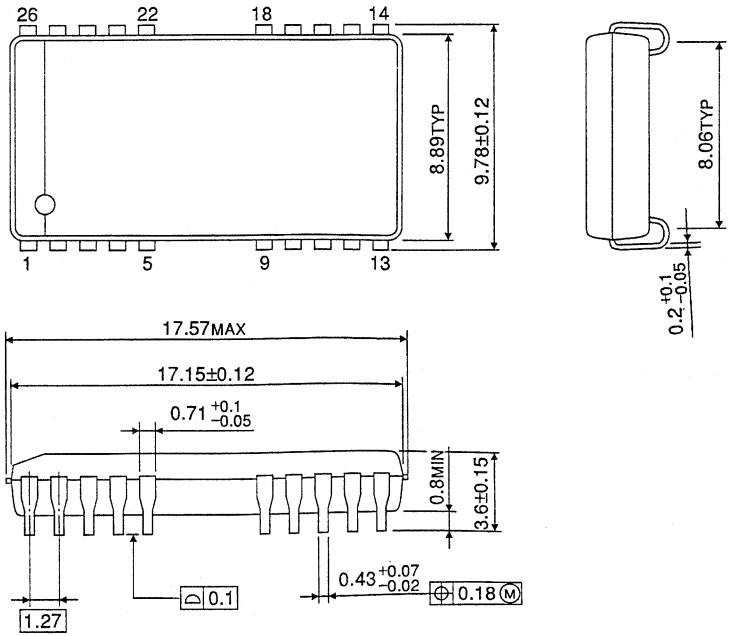


DIP28-P-300B



Unit in mm

SOJ26-P-350



SOJ28-P-300A